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9087

SYNTHESIZED SIGNAL GENERATOR

RACAL-DANA

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RACAL

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Synthesized Signal Generator 9087.

'POZIDRIV' SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trademark of G.K.N. Screws and Fasteners. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools.

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on colored paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

MOS ELECTRONIC DEVICES

This unit contains MOS devices, and care should be taken to avoid static discharge damage.

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SECTION 1 TECHNICAL SPECIFICATION

FREQUENCY

Range 10kHz to 1.3GHz (1300.000000MHz).

Resolution 1Hz throughout entire frequency range.

Frequency Accuracy Same as reference oscillator.

Reference Oscillator INTERNAL –

Standard – Aging rate 3×10^{-9} per day after 3 months continuous operation. Warm up 6 minutes to $\pm1\times10^{-7}$. Temperature stability $\pm3\times10^{-9}$ per °C from 0°C to +45°C.

Option 04B – Aging rate 5×10^{-10} per day after 3 months continuous operation. Warm up 20 minutes for $\pm1\times10^{-7}$. Temperature stability $\pm6\times10^{-10}$ per °C from −10°C to +45°C.

Option 04L5 – Aging rate 1×10^{-9} per day. Warm up 30 minutes to $\pm1\times10^{-7}$. Temperature stability 4×10^{-9} for change from 0°C to +50°C.

EXTERNAL – Any 10MHz ±100Hz frequency standard at a level between 0.1V and 5V rms into 50Ω nominal.

Reference Output 10MHz sinewave at 0dBm ±2dB from BNC socket on rear panel. Output impedance 50Ω nominal.

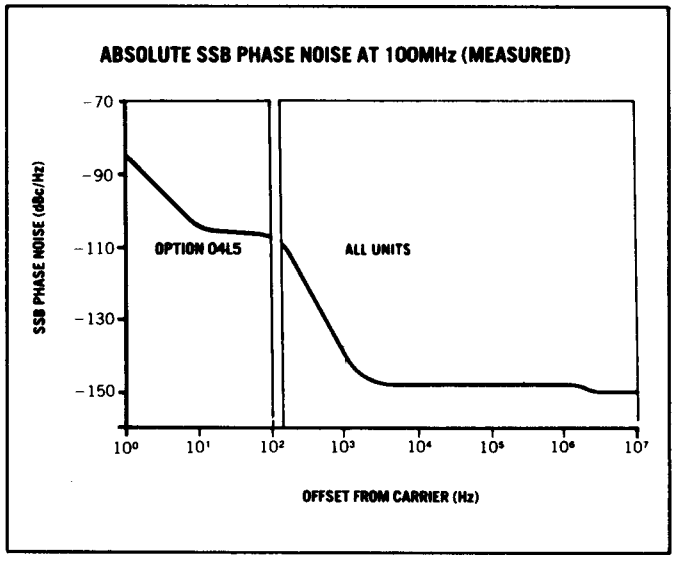
Switching Speed The total time to change frequency depends upon the method of programming. The table below gives times for any frequency change to be within 100Hz of final frequency.

Mode	Processor Time	Settling Time	Total Switching Time	Maximum Repetition Rate
Deferred	12.5mS	0.4mS	12.7mS	80/Sec
Immediate	11.8mS	0.4mS	12mS	85/Sec
Fast Learn	0.47mS	0.4mS	0.87mS	1500/Sec
DFA	0.15mS	0.4mS	0.4mS	2500/Sec

SPECTRAL PURITY

	Frequency Range			
	0.01-100MHz	**100-325MHz**	**325-650MHz**	**650-1300MHz**
SSB phase Noise [1] **3kHz to 1MHz offset from carrier (AM & CW modes)**	−136dBc/Hz	−142dBc/Hz	−136dBc/Hz	−130dBc/Hz
SSB broadband noise floor (≥ + 13dBm O/P level)	−150dBc at > 5MHz offset	−150dBc at > 2.5% offset		
Residual FM in 300kHz bandwidth	0.5Hz rms	0.25Hz rms	0.5Hz rms	1Hz rms
Spurious Signals >3kHz off carrier	−90dBc	−97dBc	−91dBc	−85dBc
Power Line related and microphonically generated (measured) [2]	−82dBc	−82dBc	−76dBc	−70dBc
Harmonics typically (≤ + 13dBm)	< −35dBc			< −30dBc
Sub-Harmonics	None			

1 Typical Absolute (includes residual and reference oscillator noise).
2 At 50Hz may be 3dB higher.



Absolute SSB Phase Noise (dBc/Hz) with Option 04L5 (Measured)

Offset From Carrier	Carrier Frequency		
	100MHz	**500MHz**	**1GHz**
1Hz	−84	−70	−64
10Hz	−104	−90	−84
100Hz	−107	−93	−87
1kHz	−139	−125	−119

OUTPUT

Range Variable from +19dBm to −140dBm. (2V to 0.0224μV rms into 50Ω).

Resolution 0.1dB.

Flatness ±0.4dB from 10kHz to 650MHz.
±0.7dB from 650MHz to 1300MHz.
(above figures referenced to 400MHz).

Absolute Level Accuracy into 50 Ω

Output Level	Frequency Ranges	
	10kHz to 650MHz	650MHz to 1300MHz
+13dBm to −37dBm	±0.6dB	±1.0dB
−37dBm to −120dBm	±1.0dB	±1.8dB
−120dBm to −140dBm	±1.5dB	±2.3dB

Notes 1. applicable at 23°C±5°C.
2. for 0° to 55°C add ±0.8dB to above figures.
3. absolute level accuracy includes flatness, attenuator error, detector error, measurement uncertainty and SWR and is valid in all operating modes.

Impedance 50 Ω nominal.

SWR

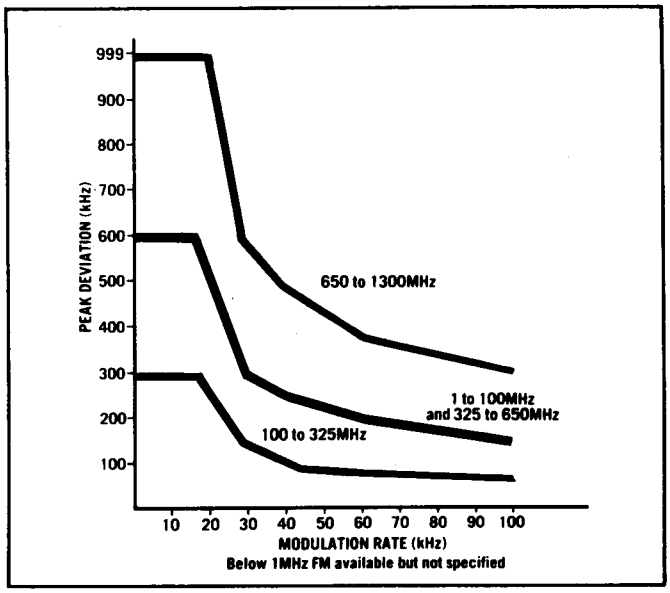
Output Level	≤500MHz	>500MHz
3dBm to 19dBm	1.6:1	1.8:1
<3dBm	1.2:1	1.3:1

Protection The output is protected against reverse power inputs up to 1W.
Reverse Power Protection Unit (RPPU) is available to protect against reverse power up to 50W.
See Option 11.

Level Switching Times 10mS to 50mS from last command statement to stable output, dependent on level change.

FREQUENCY MODULATION

Peak Deviation See below:−

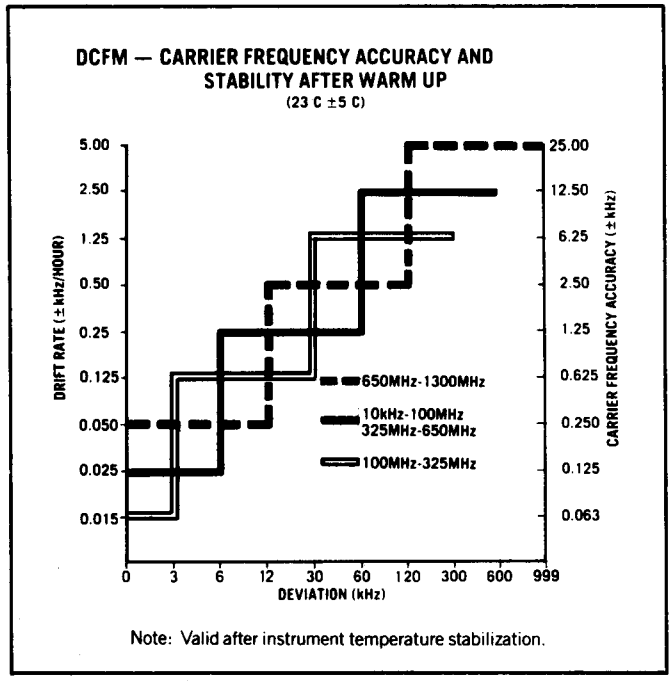


Resolution 3 digit resolution to minimum of 10Hz.

Accuracy (1kHz rate) ±5% of reading or 20Hz (whichever is greater).

Modulation Bandwidth (3dB) AC Coupled: 20Hz to 100kHz.
DC Coupled: dc to 100kHz.

Input Level AC Coupled: Any level between 0.56V and 5.6V (peak to peak) gives specified accuracy.
DC Coupled: 1.414V peak gives calibrated display.
Input impedance: 600 Ω nominal.



Note: Valid after instrument temperature stabilization.

Distortion (1kHz rate) <3% at maximum deviation.
<1% at 50% maximum deviation.
<0.3% at 75kHz deviation from 88 to 108MHz carrier frequency.

Incidental AM on FM <0.2% (−60dBc) for deviations of 20kHz at 1kHz rate.

AMPLITUDE MODULATION

Modulation Depth 0 to 99% up to +13dBm reducing to zero at +19dBm.

Resolution 1%.

Accuracy (1kHz rate) ±2% of reading ±3% AM below 80%.
Note:- Up to +13dBm the variation of modulation depth with carrier amplitude is less than ±0.5% AM, for VOR and ILS operation.

Modulation Bandwidth

Frequency Range	Modulation Bandwidth (3dB)	
1.5–1300MHz	AC	20Hz–20kHz
	DC	dc–20kHz
0.4–1.5MHz	AC	20Hz–5kHz
	DC	dc–5kHz
10kHz to 400kHz	AC	20Hz–0.1kHz
	DC	dc–0.1kHz

Distortion (1kHz rate) < 1.5% up to 30% AM
< 3% up to 80% AM

Incidental Phase Modulation (1kHz rate) < 0.1 radian at 30% AM

Input Level
AC Coupled: Any level between 0.56V and 5.6V (peak to peak) for specified accuracy.
DC Coupled: 1.414V peak gives calibrated display.
Input impedance: 600Ω nominal.

PHASE MODULATION

Phase Deviation 5 radians maximum above 60kHz carrier frequency.

Resolution 0.01 radian.

Modulation Bandwidth (3dB) 20Hz to 10kHz.

Accuracy (1kHz rate) ±10%.

Distortion (1kHz rate) < 3% at maximum phase deviation.

Input Level
AC Coupled: Any level between 0.56V and 5.6V (peak to peak) gives specified accuracy.
Input impedance: 600Ω nominal.

PULSE MODULATION

Rise and Fall Times 40nS(10%–90%).

Minimum Pulse Width 200nS

Pulse Repetition Rate

Carrier Frequency	AC	DC
10-1300MHz	20Hz-2.5MHz	dc-2.5MHz
0.01-10MHz	Available but not specified	

On/Off Ratio > 50dB (10MHz to 750MHz).
> 35dB (750MHz to 1300MHz).

Input Level
AC Coupled: 2.0V peak to peak.
DC Coupled: Carrier off below +0.9V threshold.
Carrier on above +1.7V threshold.
Input impedance: 16k Ω nominal.

Output Level Accuracy remains valid during pulse on.

Indication Front panel annunciator.

Specification valid for "Off" periods <25mS.

INTERNAL MODULATION SOURCES

Frequencies 400Hz, 1kHz.

Frequency Accuracy Same as reference oscillator.

Distortion < 1% Total Harmonic Distortion.

Outputs 2V rms ± 0.5dB emf from 600Ω.
Rear panel BNC connectors.

DIGITAL SWEEP

Sweep Limits Variable from 10kHz to 1300MHz with 1Hz resolution.

Step Size Variable from 1Hz to 1299.99MHz with 1Hz resolution.

Sweep Speed Four selectable dwell times: 2mS/step, 20mS/step, 200mS/step and 1S/step nominal.

NON-VOLATILE MEMORY

Function Allows storage of complete front panel settings of frequency, output level and modulation.

Number of Stores 33.(100 with Option 10)
Location 00 is used to store instrument status at switch-off or power interruption.

Memory Retention 30 days minimum at +40°C with instrument unpowered.

REMOTE PROGRAMMING

GPIB Interface IEEE=STD=488, 1978.

Functions Controlled All front panel functions except line power switch.

Status Indication SRQ, Talk, Listen and Remote Annunciators.

Interface Functions The interface contains the following IEEE/IEC defined "interface functions" subsets.

GPIB Subset	Description	Applicable Capability
SH1	Source Handshake	Complete Capability
AH1	Acceptor Handshake	Complete Capability
T6	Talker	Complete except talk only 1. Basic talker 2. Serial poll 3. Unaddress if MLA
TEϕ	Extended Talker	None
L3	Listener	Complete Capability 1. Basic Listener 2. Listen only mode 3. Unaddress if MTA
LEϕ	Extended Listener	None
SR1	Service Request	Complete Capability
RL1	Remote/Local	Complete Capability 1. REN – Remote Enable 2. LLO – Local Lockout 3. GTL – Go to Local
PPϕ	Parallel Poll	None
DC1	Device Clear	Complete Capability 1. DCL – Device Clear 2. SDC – Selected Device Clear
DTϕ	Device Trigger	None
Cϕ	Controller	None
E1	Open Collector Bus Drivers	—

Auxiliary Control Auxiliary controls are provided via rear panel 50-way connector.

Functions controlled
1. Step Up/Step Down with selectable debounce by contact closure to ground or negative edge triggered TTL compatible signal.
2. DFA provides access to microbus for remote control.

GENERAL

Operating Temperature 0°C to + 55°C.

Storage Temperature −40°C to +70°C (memory retention not guaranteed below −20°C or above +65°C).

Humidity 95% RH at +40°C.

EMC Meets radiated and conducted limits of MIL-STD 461A methods RE02 and CE03, and VDE 0871.

Carrier Leakage The voltage induced in a two turn 1 inch diameter loop 1 inch away from any surface is less than 0.5μV measured into a 50Ω receiver.

Power Requirements

Voltage Ranges	100 (90 to 110) V 120 (103 to 127) V 220 (193 to 237) V 240 (207 to 253) V AC
Frequency	45-66Hz. (For 400Hz operation consult factory).
Consumption	Approximately 320VA.

OPTIONS

01	Rear Panel connectors. Alternative type N carrier output and BNC modulation inputs available on rear panel.
04B	High Stability Frequency Standard Racal-Dana model 9421: Aging rate 5×10^{-10} per day after 3 months continuous operation.
04L5	Low Noise Frequency Standard. Aging rate 1×10^{-9} per day.
10	100 Store Non-Volatile Memory.
11	RPPU — Output protected up to 50 watts from a 50Ω source over the frequency range 10kHz to 1.3GHz or to 50V dc. Insertion loss: ±0.2dB (≤650MHz) +0.2dB to −0.8dB (>650MHz) Output SWR (typical): ≤500MHz 1.3:1 (<3dBm) >500MHz 1.5:1 (<3dBm).
60	Rack Mounting Kit (fixed).
65	Rack Mounting Kit (slides).

ORDERING INFORMATION

9087 Synthesized Signal Generator.

Options

01 Rear Panel Connectors.
04B 9421 Frequency Standard.
04L5 Low Noise Frequency Standard.
10 100 Store Memory (11-1584).
11 Reverse Power Protection Unit.
60 Rack Mounting Kit (fixed) 11-1576.
65 Rack Mounting Kit (slides) 11-1577.

ACCESSORIES

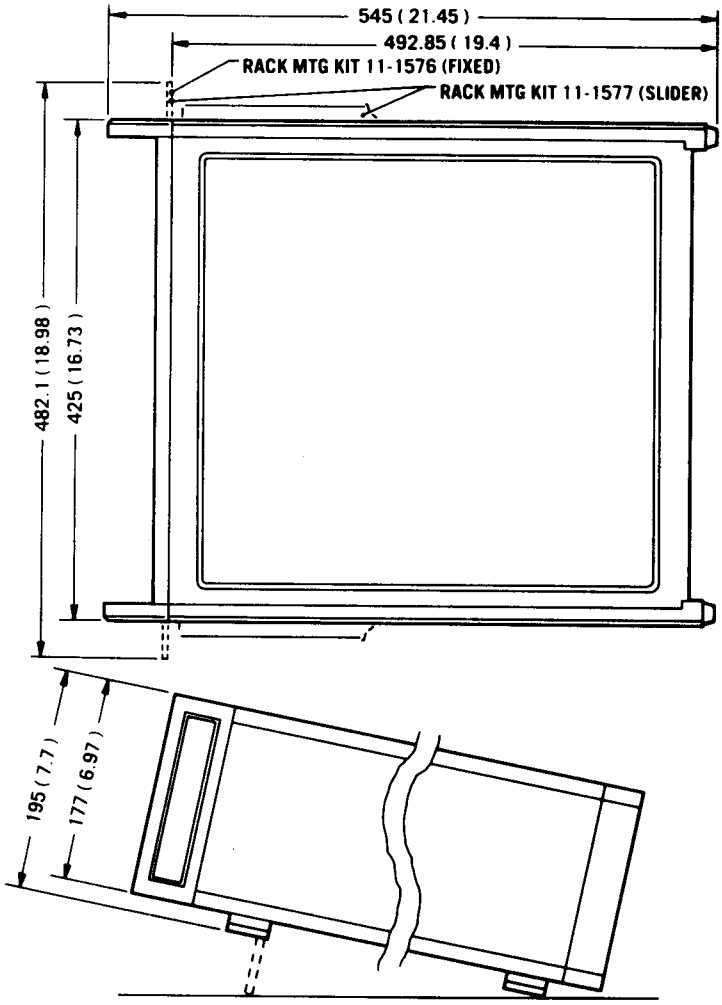
A comprehensive range of accessories is available for the 9087 including:-

23-3174 50-75Ω Adaptor (10dB attenuation).
23-3190 N-BNC Adaptor.
11-1579 Service Support Kit. Maintenance Manual.

MECHANICAL

Dimensions (Max.) In millimeters (inches).

Weight Approximately 25kg (55lbs).



SECTION 2 GENERAL DESCRIPTION

2.1 INTRODUCTION

2.1.1 The Racal-Dana signal generator Model 9087 is designed primarily for the testing of communication equipment over the frequency range from 10 kHz to 1.3 GHz. The RF output is phase-locked to the frequency standard, the wide frequency range being obtained by the use of a multiloop synthesizer. The instrument is microprocessor controlled, and combines versatility with ease-of-control.

2.2 RF TUNING

2.2.1 Tuning may be effected in one of five ways. These are:

(a) Numeric keyboard. The required frequency is set directly.

(b) Step-up and step-down keys. The displayed frequency is changed in steps. The step size may be one of three preset values, or an operator-set value.

(c) Spinwheel. The displayed frequency changes in steps as the spinwheel is rotated. Again, the step size may be one of three preset values or an operator-set value. The use of the spinwheel, particularly with a small step size, affords all the advantages of analog tuning while retaining the stability of a synthesized system. A HOLD control is provided to isolate the spinwheel to prevent accidental changing of the frequency set.

(d) GPIB. An internal interface is fitted.

(e) Direct frequency access (DFA). The required frequency may be set by applying suitable control signals directly to the microprocessor data bus to a rear-panel socket. The use of this method permits extremely rapid changes of frequency to be made. A special interface is required. Full details may be obtained from Racal-Dana Instruments.

2.2.2. The frequency set is displayed on a 10-digit, dot-matrix LED display, affording 1-Hz resolution throughout the frequency range of the instrument. The decimal point is fixed, and leading zeros are suppressed.

2.3 FREQUENCY SWEEP

2.3.1 The 9087 incorporates a frequency-sweep facility which permits the output frequency to be swept, in steps, between two operator-selectable frequencies. The step size can be selected by the operator, and four preset step rates are available.

2.4 RF OUTPUT

2.4.1 Automatic levelling maintains the output level within ±0.4 dB for output frequencies up to 650 MHz, and within ±1.0 dB for output frequencies in the range from 650 MHz to 1.3 GHz, relative to the 50 MHz level.

2.4.2 The output-level range is from +19 dBm to -140 dBm into 50 Ω. The level may be set by means of a numeric keyboard, or the set value may be stepped up or down using either the step keys or the spinwheel. The step size may be one of three preset values, or an operator-set value.

2.5 MODULATION FACILITIES

2.5.1 Amplitude, pulse, frequency, and phase modulation facilities are provided. Two internal-modulating frequencies, locked to the frequency standard, are provided, and external-modulating sources may also be used. Details of the permissible range of modulating frequencies, and of the modulation depths and peak deviations which can be obtained, are to be found in Section 1 of this manual.

2.5.2 Amplitude or pulse modulation may be applied simultaneously with frequency or phase modulation. Either or both of the internal-modulating sources, or a combination of internal and external sources may be used.

2.6 FRONT-PANEL SETTING STORAGE

2.6.1 A non-volatile memory allows the storage of up to 33 (100, if the 100-location memory option is fitted) complete sets of front-panel control settings. These may then be recalled when required. The recalled data may be implemented immediately, or may be displayed for checking before the instrument output is reset. This facility allows the contents of the store to be examined without affecting the output of the instrument.

2.6.2 An exchange facility allows the contents of any two store locations to be exchanged without affecting the output of the instrument.

2.6.3 On switching off, the current front-panel control settings are stored automatically. On switching on again, these settings are immediately implemented. An initialization program is also provided to set the instrument to a known state.

2.7 ERROR INDICATIONS

2.7.1 Certain errors in the operation of the instrument will result in the flashing of a LED-error indicator and the generation of a service request (SRQ) via the GPIB interface. The errors which can be detected are each given a two-digit code, which can be displayed. The nature of the error can then be established by reference to the pull-out information card beneath the instrument or to Section 4 of this manual.

2.8 DIAGNOSTIC CHECKS

2.8.1 Several points in the instrument's circuits are monitored for possible malfunction. The detection of a fault is indicated by the generation of an error indication. A digit in the numeric displays will flash to indicate the location of the fault.

2.8.2 In the event of overheating, the instrument is switched automatically to the standby condition, with only the frequency standard and the microprocessor system active.

2.9 SPECIAL FUNCTIONS

2.9.1 A number of special functions are available to the operator. Details are given in Section 4 of this manual.

2.10 OUTPUT PROTECTION

2.10.1 The RF output will withstand the accidental application of reverse-RF power at levels up to 1 W.

2.10.2 Protection against reverse powers of up to 50 W is given by the internally mounted, reverse-power-protection-unit option. This isolates the RF output socket, and sounds an audible alarm, when reverse powers are applied above the threshold level. The device latches in the tripped state.

2.11 GPIB INTERFACE

2.11.1 An internally mounted interface to the IEEE-488-GPIB is provided. This enables all the instrument functions, except the line power switching and frequency standard changeover, to be remotely controlled. An adapter to provide compatibility with the IEC 625-1 bus is available as an optional accessory.

2.11.2 Control via the GPIB may be exercised in one of three ways. These are:

(a) Immediate Mode Control, in which each data byte accepted by the 9087 from the bus is processed before the next byte is accepted. This provides the shortest delay in completing the resetting of the 9087's output following a data entry made on a controller keyboard.

(b) Deferred Mode Control, in which the complete data string is accepted from the bus and stored before processing is commenced. The use of the bus is therefore limited to the data transfer time, and better utilization of the bus is possible at the cost of a small increase in the total time taken to vary the 9087's output parameters.

(c) Learn Mode Control, in which data strings related to particular settings of the 9087's output are generated in the 9087 and stored in an external memory. When a data string is fed back to the 9087 as an addressed command, the output parameters will be set to the related values. This provides a significant saving in time when compared with keyboard control, and, by feeding back a succession of data strings, the 9087 may be stepped rapidly through a number of different output-parameter patterns. Two lengths of data string are available, the longer controlling the full range of output parameters and the other controlling frequency only. The longer data string may also be used to monitor the instrument's settings. This may be found useful when the 9087 is used in operator-interactive systems.

2.12 EXTERNAL STEP SWITCHES

2.12.1 External step-up and step-down switches may be fitted by the user to provide remote control of the instrument's incremental-control function.

2.13 MAINTENANCE

2.13.1 It is recommended that customers take advantage of the repair and calibration service offered by Racal-Dana Instruments and their agents. For customers wishing to carry out their own servicing, a comprehensive Maintenance Manual is available from Racal-Dana Instruments. When ordering, the serial number of the instrument for which the manual is required should be quoted.

SECTION 3 PREPARATION FOR USE

3.1 PACKAGING

3.1.1 Unpack the instrument carefully to avoid unnecessary damage to the factory packaging.

3.1.2 If the instrument is to be returned to Racal-Dana Instruments for calibration or repair, the original packaging should be used whenever possible. If this is not possible, a strong shipping container should be used. This must be fitted with internal packing capable of preventing movement of the instrument within the container.

3.2 POWER SUPPLY

3.2.1 AC-VOLTAGE RANGE SETTING

3.2.1.1 The supply-voltage setting is varied by changing the position of a small printed circuit board located under the fuse on the rear panel. The setting in use can be seen through the clear plastic fuse cover.

3.2.1.2 If it is necessary to change the voltage range proceed as follows:

(a) Switch the instrument off, and remove the line power socket.

(b) Slide the clear plastic fuse cover to the left, to expose the fuse.

(c) Pull the lug marked FUSE PULL out and to the left. This will remove one end of the fuse from its holder. Remove the fuse.

(d) Using a pair of snipe-nosed pliers, pull out the voltage-setting board from beneath the fuse holder.

(e) Reinsert the board so that the required voltage range can be read the correct way up, when viewed from above, looking at the rear of the instrument.

(f) Push the lug marked FUSE PULL back into position.

(g) Insert the correct fuse for the range selected into the fuse holder.

(h) Slide the clear plastic cover to the right until it is clear of the line power plug. Insert the line power socket.

3.2.2 LINE FUSE

3.2.2.1 Check that the line fuse rating is correct for the local AC supply voltage. The fuse is a ¼ in x 1¼ in glass cartridge, anti-surge type. The Racal-Dana part numbers for replacement fuses are:-

90V to 132V supply/4 AT: 23-0061
198V to 264V supply/2 AT: 23-0036

3.2.3 DC FUSES

3.2.3.1 Check that the DC fuses are serviceable and of the correct rating. The fuses are mounted beneath a hinged cover on the rear panel of the instrument. The cover is released by removing the two screws in the upper and lower left-hand corners. The fuses are numbered FS1 to FS9 from top to bottom, and are all of the 5 mm x 20 mm, glass cartridge, quick-action type. The ratings and part numbers are:

Fuse Number	Rating	Part Number
1	2 A	23-0008
2	2 A	23-0008
3	2 A	23-0008
4	1.5 A	23-0007
5	3 A	23-0009
6	3 A	23-0009
7	3 A	23-0009
8	2 A	23-0008
9	0.5 A	23-0004

3.2.4 POWER CORD

3.2.4.1 The power cord must be fitted with a suitable connector in accordance with the standard color code.

	European	American
Live	Brown	Black
Neutral	Blue	White
Earth(Ground)	Green/Yellow	Green

3.3 FREQUENCY STANDARD

3.3.1 If it is intended to use an external frequency standard, this should be connected at the EXT. STANDARD I/P socket on the rear panel. The STANDARD switch on the rear panel should be set to EXT.

3.3.2 If the internal frequency standard is to be used, ensure that the STANDARD switch is set to INT.

3.3.3 If it is intended to use the 10-MHz signal derived from the frequency standard, make the necessary connection at the rear-panel, 10-MHz STANDARD OUTPUT socket.

3.4 EXTERNAL STEP SWITCHES

3.4.1 If external control of the step-up and step-down functions is required, connect the external switches to the rear-panel AUXILIARY CONTROL connector. The switches should be connected from pin 28 (for step up) and pin 29 (for step down) to 0V at pin 30. The mating connector required is a plug, 3M type 3564-1001, Racal-Dana part number 23-3320. Contact closure initiates the step.

3.4.2 Internal contact debouncing is provided. This is enabled on switching-on or following initialization, but can be disabled using special function 06 and enabled using special function 05. The procedure for using the special functions is given in Section 4.

3.5 BATTERY CHARGING

3.5.1 When the instrument is ready for use, the state of charge of the memory battery should be checked. Connect the instrument to the AC supply and set the LINE switch to ON. If the BATTERY LOW indicator lights, the instrument should be left switched on (switched to the standby condition if not required for use) until the indicator is extinguished. A full charge-cycle takes approximately 14 hours.

3.5.2 If the BATTERY LOW indicator lights, the front-panel control-setting patterns stored in the memory may have been corrupted, and should be checked before use, using special function 76.

3.6 OPERATOR'S CHECKS

3.6.1 FUNCTIONAL CHECKS

3.6.1.1 The procedure which follows checks all the instrument's functions to establish whether they perform normally. The procedure does not verify absolute accuracy. Detailed performance tests are given in Section 7 of the maintenance manual.

3.6.1.2 The recommended test equipment is:

(a) Frequency Counter, Racal-Dana Model 9514 with Option 42.

(b) Spectrum Analyzer, Hewlett-Packard Model 141T fitted with RF section 8554B and IF section 8552B.

Other equipment of similar specification may be used.

3.6.1.3 Connect the 9087-under-test to the frequency counter as shown in Fig. 3.1. If a frequency counter other than the 9514 is used, it is permissible to use the frequency standard in the 9087 as the reference. In this case the frequency counter should be set to operate from an external standard input, which should be provided from the 10-MHz STD OUT socket of the 9087.

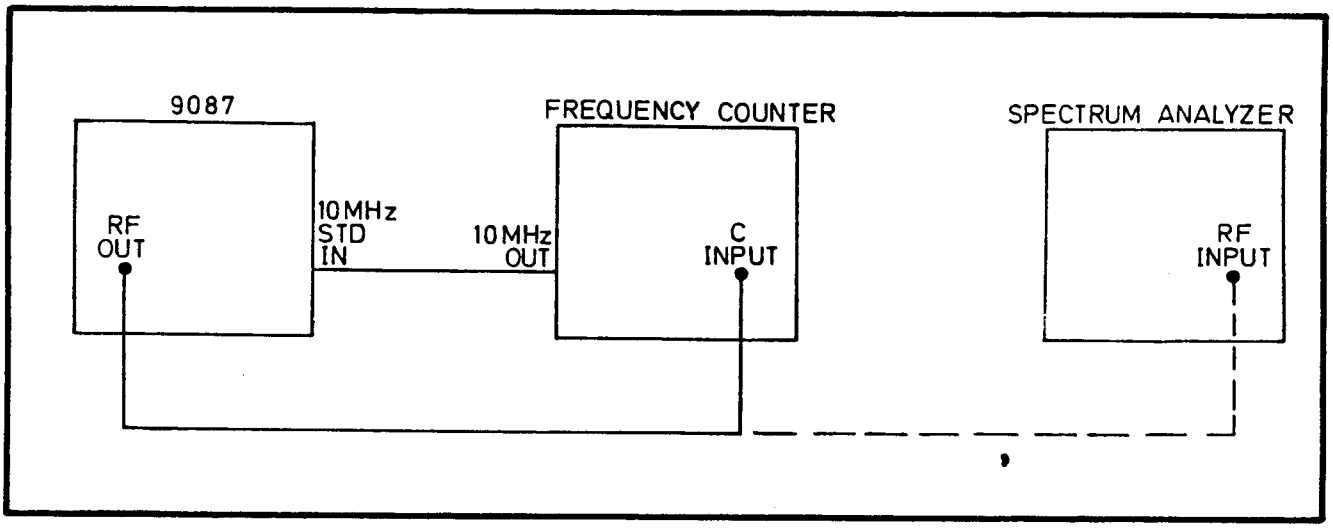


Fig 3.1 Functional Check Connections

3.6.1.4 Set the 9087's RF output amplitude to -10.0 dBm and frequency to the values in Table 3.1. The counter reading should be the frequency that is set plus the resolution error for the counter being used (for 9514, ± 1 Hz).

TABLE 3.1

Check Frequencies

MHz
0.01
0.1
1.0
10.0
1000.0

3.6.1.5 Set the 9087's frequency to 111.111 111 MHz. Set the step size to 111.111 111 MHz. Select STEP, and use the STEP UP key to step in turn the displayed frequency to each value shown in Table 3.2. Check that the frequency counter indicates the frequency on the 9087 display at each step. Repeat the test using the STEP DOWN key.

TABLE 3.2

Check Frequencies

MHz
111.111 111
222.222 222
333.333 333
444.444 444
555.555 555
666.666 666
777.777 777
888.888 888
999.999 999

3.6.1.6 Set the 9087 to sweep from 1 to 1300 MHz in 1-MHz steps at 20 ms/step. Set the 9087's RF output amplitude to +0 dBm. Set the spectrum analyzer to a center frequency of 650 MHz with 1250 MHz scan, fast scan rate, and a +10 dBm reference level.

3.6.1.7 Connect the 9087's RF OUTPUT to the RF INPUT of the analyzer, using low-loss RF cable with Type N connectors. The display should be a continuous sweep (that is, no jumps or gaps). Harmonics can be seen over most of the sweep and should be more than 35 dB below the carrier up to 650 MHz.

3.6.1.8 Stop the 9087's sweep and set the output amplitude to +0 dBm. Tune the 9087 over the whole frequency band in 10-MHz steps, using the spinwheel. Check that the displayed level does not vary more than 2 dB +analyzer flatness, and that there are no discontinuities in the reponse.

3.6.1.9 Tune the 9087 and analyzer to 150 MHz. Set the analyzer ref level to +10 dBm. Set the 9087's output level to 10 dBm. Using the spinwheel, reduce the output amplitude in 0.1 dB steps to 0 dBm, then in 3 dB steps down to -66 dBm. Note that the level on the analyzer display decreases smoothly in appropriate steps without jumps or reversals.

3.6.1.10 Set the 9087's output level to +0 dBm, frequency to 650 MHz, and FM to 100-kHz peak deviation and 1 kHz rate (INT 1k). Set the spectrum analyzer to 650 MHz center frequency, 50 kHz span/division and a 0dBm reference level. The analyzer display should be similar to Figure 3.2.

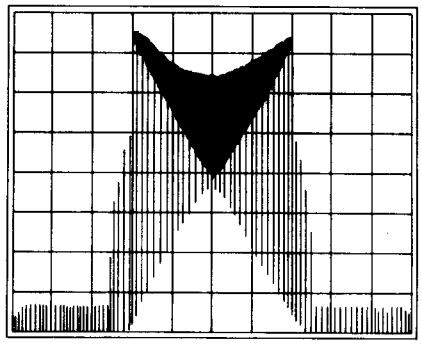


Fig 3.2 Spectrum Analyzer Display

3.6.1.11 Using the spinwheel, slowly decrease FM deviation to zero. The deviation displayed on the analyzer should decrease smoothly.

3.6.1.12 Set the 9087 to 50% AM at a 400 Hz rate (INT 400). Set the analyzer to zero span and fine tune the center frequency for maximum level of the demodulated signal. Set the analyzer to linear amplitude mode. The demodulated signal should be a sine wave with a 2.5 ms period (that is, 400 Hz).

3.6.1.13 Set the 9087 to INT 1k (modulation rate). The period of the demodulated signal should become 1 ms (that is, 1 kHz).

3.6.2 GPIB CHECK

3.6.2.1 Introduction

3.6.2.1.1 The procedure which follows checks the ability of the 9087 to process or send GPIB messages. Each test may be performed separately, if required.

3.6.2.1.2 The validity of these checks is based on the following assumptions:

(a) The 9087 operates correctly from the keyboard. This can be verified with the preceding functional check.

(b) The 9087's memory circuits are good. This is verified automatically at each turn-on.

(c) The controller properly executes GPIB operations to IEEE-488-1978.

(d) The controller-GPIB interface properly transfers the controller's instructions.

If the 9087 appears to fail any of the GPIB checks, the validity of the above assumptions should be confirmed before servicing the 9087.

3.6.2.1.3 The recommended test equipment is the Hewlett-Packard HP-85 GPIB controller, with GPIB I/O ROM in the drawer. It is assumed that the select code of the controller I/O is 7 and that the address of the 9087 is 19 (the address is set when the instrument leaves the factory). If any other controller or select code/address combination is used, the GPIB commands given in the following paragraphs will require modification. The controller should be connected to the 9087's GPIB interface via a GPIB cable.

3.6.2.1.4 The 9087 does not require any special control settings. However, it should be initialized at the beginning of a series of checks. This is a good step to perform also at the end of the checks and before general operation.

3.6.2.1.5 If all of these checks are successful, the instrument's GPIB interface is operating correctly. These procedures do not check that all of the device-dependent codes can be executed. However, if the 9087 works correctly from the keyboard, its memory circuits check correctly, and the GPIB interface works correctly, then there is a high probability that it will respond to all program codes.

3.6.2.2 Remote and Local Message Check

3.6.2.2.1 This check assumes that the 9087 is in the local state, a default condition at turn-on. Thus, the Remote Check precedes the Local Check. If the instrument is in the remote state (that is, its front panel REMOTE indicator is lit), switch it off and then on again.

3.6.2.2.2 Test as follows:

Action	HP-85 Code
Send the REN message true, followed by the 9087's listen address	REMOTE 719

Check that the 9087's REMOTE indicator is lit.

3.6.2.2.3 Test as follows:

Action	HP-85 Code
Send the 9087's listen address followed by the GTL message	LOCAL 719

Check that the 9087's REMOTE indicator is extinguished.

3.6.2.3 Local-Lockout and Clear-Lockout Check

3.6.2.3.1 The 9087 is put to the remote state before setting local lockout. Test as follows:

Action	HP-85 Code
Send the REN message true, followed by the 9087's listen address	REMOTE 719
Send the LLO message	LOCAL LOCKOUT 7

Check that the 9087's REMOTE indicator is lit. Operate the 9087 front-panel LOCAL key, and check that the REMOTE indicator remains lit.

3.6.2.3.2 Test as follows:

Action	HP-85 Code
Send the REN message false	LOCAL 7

Check that the 9087's REMOTE indicator is extinguished.

3.6.2.3.3 Test as follows:

Action	HP-85 Code
Send the REN message true, followed by the 9087's listen address	REMOTE 719

Check that the 9087's REMOTE indicator is lit. Operate the LOCAL key on the 9087's front panel and check that the REMOTE indicator is extinguished.

3.6.2.4 Data Message Check

3.6.2.4.1 The 9087 is put to the remote state at the commencement of the check. Test a follows:

Action	HP-85 Code
Send the REN message true, followed by the 9087's listen address	REMOTE 719
Set the 9087's status byte mask to 377. Set the data output mode to send the data string by sending the 9087's listen address followed by the device-dependent command string RS377IS	OUTPUT 719;"RS377IS"
Prepare a store to receive a 27-byte data string	DIM Z$ 27
Send the 9087's talk address. Store the 27-byte data string in the prepared store. Send the UNTALK message true when the string has been stored.	ENTER 719 USING "#,27A";Z$
Print the contents of the store.	DISP Z$

Check that the store contains 00,00,00,00,00,00,377,000 followed by carriage return and line feed.

3.6.2.4.2 Test as follows:

Action	HP-85 Code
Set the 9087's status byte mask to all 0's by sending the device-dependent command string RS000	OUTPUT 719;"RS000"
Prepare a store to receive a 27-byte data string	DIM M$ 27
Send the 9087's talk address. Store the 27-byte data string in the prepared store. Send the UNTALK message true when the string has been stored.	ENTER 719 USING "#,27A";M$
Print the contents of the store	DISP M$

Check that the store contains 00,00,00,00,00,00,000,000 followed by carriage return and line feed.

3.6.2.5 SRQ and Status Btye Check

3.6.2.5.1 Test as follows:

Action	HP-85 Code
Send the REN message true, followed by the 9087's listen address and the device-dependent command string RS300	REMOTE 7 OUTPUT 719;"RS300"
Set the 9087 to local control by either (a) sending the REM message false (b) sending the GTL message (c) operating the LOCAL key on the 9087's front panel	LOCAL 719

Activate special function 44, using the 9087's front-panel controls. Check that the SRQ indicator lights.

3.6.2.5.2 Test as follows:

Action	HP-85 Code
Store the status of the GPIB interface of the controller in binary form.	STATUS 7,2;5
Print the status of the SRQ line	DISP "SRQ =";BIT (S,5)

Check that the SRQ message has been sent true (SRQ status bit at 1 or SRQ line $\leqslant$0.8V).

3.6.2.5.3 Test as follows:

Action	HP-85 Code
Conduct a serial poll and store the status byte of the 9087	R = SPOLL (719)
Print the contents of the store	DISP "R=";R

Check that the SRQ indicator on the 9087's front panel is extinguished when the serial poll is made. The value of R should be 192 (store contents should be 11000000),

3.6.2.6 Device Clear and Selected Device-Clear Check

3.6.2.6.1 The 9087 is put to the remote state with the frequency at a frequency other than 100 MHz at the commencement of the test. Test as follows:

Action	HP-85 Code
Send the REN message true, followed by the 9087's listen address and the device-dependent command string FQ555MZ	REMOTE 7 OUTPUT 719;"FQ555MZ"
Send the DCL message true	CLEAR 7
Reset the 9087's frequency by sending the 9087's listen address and the device-dependent command string FQ555MZ	OUTPUT 719;"FQ555MZ"
Send the SDC message true	CLEAR 719

Check that the 9087's frequency changes from 555 MHz to 100 MHz for both the DCL and SDC messages

3.6.2.7 IFC Check

3.6.2.7.1 The 9087 is put to the remote state at the commencement of the test. A dummy command string is sent to put the 9087 into the listener active state (LACS). Test as follows:

Action	HP-85 Code
Send the REN message true followed by the 9087's listen address	REMOTE 719
Send a dummy command string	OUTPUT 719
Send the IFC message true	ABORTIO 7

Check that the REMOTE indicator on the 9087 lights after the first step and the LISTEN indicator lights when the dummy command string is received. Check that the LISTEN indicator is extinguished when the IFC message is received.

3.7 FITTING THE FIXED RACK MOUNTING KIT 11-1576

CAUTION: THE RACK MOUNTING KIT 11-1576 PROVIDES SUPPORT FOR THE 9087 AT THE FRONT OF THE RACK ONLY. BECAUSE OF THE WEIGHT OF THE INSTRUMENT, ADDITIONAL SUPPORT MUST BE PROVIDED AT THE REAR OF THE 9087 USING HANGERS SUITED TO THE RACK IN USE.

3.7.1 The kit contains a pair of mounting brackets and four screws. The method of fitting the kit is shown in Fig. 3.3. The fitting procedure is as follows:

(a) Switch off the instrument and the AC supply. Remove the line power socket.

(b) Stand the instrument upside down on a firm bench.

(c) Remove the two screws from each of the plastic moldings at the rear corners of the instrument. Remove the moldings.

(d) Slide the bottom cover towards the rear of the instrument by about 1 inch, and lift the cover off.

(e) Remove the bench feet from the bottom cover by removing the retaining screw from each foot. Replace the bottom cover.

(f) Remove the side trim panels by sliding them to the rear of the instrument. Replace and secure the plastic moldings removed in (c).

(g) Remove the two screws securing the handle at one side of the instrument. Do not remove the handle.

(h) Position a bracket from the kit at the side of the instrument, so that the two holes in a flange are positioned over the holes for the handle-securing screws.

(j) Secure the handle and bracket, using two of the countersunk-headed screws from the kit.

(k) Repeat (g) to (j) at the other side of the instrument.

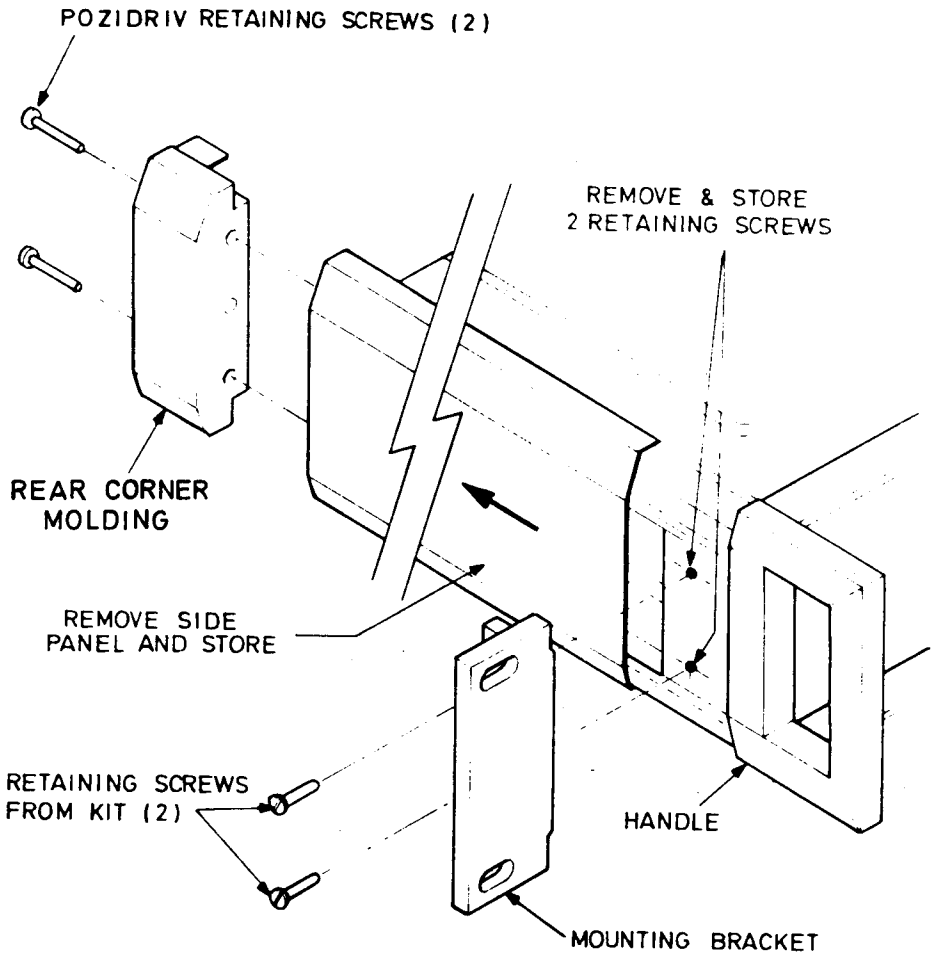


Fig. 3.3 Fitting the Rack Mounting Kit 11-1576

SECTION 4 OPERATING INSTRUCTIONS

4.1 INTRODUCTION

4.1.1 The instrument should be prepared for use in accordance with the instructions given in Section 3. If the instrument is being used for the first time, or at a new location, pay particular attention to the setting of the supply-voltage range-selector.

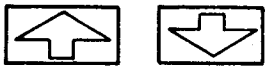
4.2 DESCRIPTION OF CONTROLS, INDICATORS AND CONNECTORS

4.2.1 Each group of controls or connectors described is numbered to correspond with the indicators on Fig. 4.1 (front panel) or Fig. 4.2 (rear panel). With the exception of the LINE switch, the front-panel keys are of the pressure-sensitive membrane-type. The numeric indicators are of the LED dot-matrix type.

4.2.2 FRONT PANEL ITEMS

Reference	Indicators, Controls and Connectors	Functions
①	GPIB Indicators	
	REMOTE	ON: Indicates that the controller has placed the instrument in the remote operation mode.
	LISTEN	ON: Indicates that the instrument is programmed by the controller to function as a listener on the GPIB or is set to LISTEN ONLY.
	TALK	ON: Indicates that the instrument is programmed by the controller to function as a talker on the GPIB.
	SRQ	ON: Indicates that the instrument is transmitting a service request (interrupt) to the controller in systems operation.
②	RELATIVE	ON: Indicates that the frequency displayed is either a +ve or -ve offset from a previously set reference frequency.
③	Frequency Display	A 10-digit display indicating frequency parameters or status codes and error information.
④	STEP SIZE	ON: Indicates that the frequency displayed is the currently stored step size.

Reference	Indicators, Controls and Connectors	Functions
⑤	Modulation Display	A 3-digit display with decimal points, indicating value of modulation in %, kHz or radians.
⑥	%	ON: Indicates modulation display is displaying % AM.
	kHz	ON: Indicates modulation display is displaying kHz deviation.
	Rads	ON: Indicates modulation display is displaying phase mod in radians.
	PULSE	ON: Indicates that pulse modulation is selected. The modulation display is blanked.
	CAL?	ON: Indicates that the actual modulation may not be as displayed.
⑦	RELATIVE	ON: Indicates that the amplitude displayed is a +ve or -ve offset from a previously set reference level.
⑧	Output Amplitude Display	A $3\frac{1}{2}$-digit display indicating RF level, relative or step size in voltage units or dB. The display is also used for the special function No.
⑨	STEP SIZE	ON: Indicates that the amplitude displayed is the currently stored step size in voltage units or dB.
⑩	dB	ON: Indicates amplitude display is in dB - relative or step size.
	dBm	ON: Indicates amplitude display is in dBm (50-Ω source)
	nV, µV, mV	ON: Indicates amplitude display is in voltage units, actual output RMS into 50 Ω, step size or relative.
	dB µV	ON: Indicates amplitude display is in dB relative to 1 µV.
⑪	Memory Display	A 2-digit display indicating the memory location for front-panel setups or an error code for invalid commands/conditions.
⑫	BATT LOW	ON: Indicates memory battery voltage was low.

Reference	Indicators, Controls and Connectors	Functions
(13)	ERROR	FLASHING: Indicates an invalid command (Local or Remote) or a system hardware error.
(14)	DISPLAY ERROR CODE	Displays current error code when held in.
(15)	Memory Function - Control Keys	Keys for storing, receiving, exchanging and executing the front- panel setups in designated locations.
(16)	Spinwheel 	Rotated in either direction to control the parameters of frequency, modulation, output level and memory location.
(17)	Increment Controls FINE MEDIUM COARSE STEP HOLD	Selects preset or user-defined step sizes for spinwheel and step-up/down keys. ON: Disables spinwheel only.
(18)	Step-Up Step-Down Keys 	One press changes value of current function by the selected increment. Provides continuous stepping when held in.
(19)	Units Keys	Used to terminate and activate data entry. Also used for units conversion in amplitude mode.
(20)	Data Entry BACK SPACE	Entry of numeric values, +ve or -ve with or without decimal point for setting of all functions, special functions, or memory locations. Provided for entry correction.
(21)	FM/Phase Mod AF IN	BNC socket for external modulating signal input (FM or ØM)
(22)	HIGH	ON: External modulating signal level is too high.
(23)	LOW	ON: External modulating signal level is too low.
(24)	Modulation Primary Function Keys	Selects one of four modulation modes (Pulse, AM, FM, ØM) for further manipulation. When associated LED is on, modulation values can be altered either by keyboard entry or by the increment controls.

Reference	Indicators, Controls and Connectors	Functions
(25)	Modulation Source and Control keys with indicators	Enables/disables modulation and the source for both Pulse/AM and FM/ØM. Each column of keys is independent.
(26)	Pulse/AM Mod AF IN	BNC Socket for external modulating signal input (AM or Pulse mod)
(27)	ON OFF	ON: Indicates RF Signal available at the output socket. (Toggle-action key).
(28)	RF OUTPUT	'N' type connector (50 Ω) for RF output
(29)	AMPLITUDE	ON: Amplitude selected. Selects amplitude as the primary function. Values of Amplitude parameters can be entered via the keyboard or altered by the increment controls.
(30)	LINE	A press-on, press-off switch controlling the AC supply to the instrument.
(31)	STAND-BY	ON: Indicates instrument is in standby mode. FLASHING: Instrument has overheated and shutdown into standby mode. Toggle action. Controls standby/normal modes. In standby mode, processor and frequency standard only are active.
(32)	REL	ON: Relative mode selected. Toggle action. Selects relative mode for either frequency or amplitude. Values entered in this mode are offsets from a reference value.
(33)	INIT	Initiates the power-up check cycle and leaves instrument in a preset state.
(34)	STEP SIZE	ON: Step -size mode selected. Toggle action. Selects and displays the step-size mode for the required function (frequency or amplitude). Values cannot be entered via spinwheel.
(35)	LOCAL	Returns instrument to local control from remote GPIB control, provided Local Lockout has not been sent.

Reference	Indicators, Controls and Connectors	Functions
(36)	FREQUENCY	ON: Frequency selected. Selects frequency as the primary function. Values of frequency parameters can be entered via the keyboard or altered by the increment controls.
(37)	SPECIAL FUNCT	Key plus two digits accesses additional features, including digital sweep and diagnostic routines.
(38)	SWEEP	ON: Frequency sweeping under special function control.
(39)	START	ON: Sweep-start frequency displayed (special function 86).
(40)	STOP	ON: Sweep-stop frequency displayed (special function 87).

4.2.3 REAR PANEL ITEMS

(41)	Supply-Voltage Range Selector	This allows the selection of one of four line-voltage ranges. The range selected can be read on the selecting plate through the clear plastic cover.
(42)	Line Fuse	The fuse is a ¼ in x 1¼ in glass cartridge pattern, and should be of the anti-surge type. See paragraph 3.2.2 for ratings.
(43)	Line Power Plug	The power input plug incorporates a filter, and external supply filtering should be unnecessary.
(44)	RF Output Connector	A 50-Ω Type-N output connector may be fitted in this position as an alternative to the front-panel position.
(45)	Auxiliary Control Socket	Pins 28, 29 and 30 permit the connection of external step-up and step-down switches for the data incrementing system. The socket also provides direct access to the instrument's address and data buses. The use of a special interface in conjunction with this socket permits extremely rapid frequency changes to be made. Details may be obtained from Racal-Dana Instruments.

Reference	Indicators, Controls and Connectors	Functions
(46)	DC Fuses	The DC fuses are mounted below a hinged cover plate. The plate is released by removing the two screws at the left-hand corners.
(47)	External 10-MHz Standard Input	A BNC connector is provided to permit the connection of a 10-MHz signal from an external frequency standard.
(48)	Internal Modulation Source Outputs	The 400 Hz and 1 kHz signals from the internal modulation source are available at these BNC sockets. The signals are available regardless of whether the source is selected or modulation is enabled.
(49)	AF Input Sockets	The AF sockets for the connection of external modulation sources may be fitted in this position as an alternative to front-panel mounting.
(50)	10-MHz Standard Output	A 10-MHz signal, derived from the frequency standard in use, is available at this BNC connector.
(51)	Internal/External Frequency Standard Switch	This slide switch permits selection of the internal or external frequency standard.
(52)	GPIB Socket	This socket is wired for direct connection to the IEEE-488-bus. An adapter to permit the instrument to be used with the IEC 625-1 bus is available as an optional accessory.
(53)	Address Switches	The upper five switches allow one of 31 Listen/Talk address pairs to be selected. Putting a switch to the right represents a logic '1'. The top switch represents the least significant bit (bit 1, on DIO 1). The sixth switch, when put to the right, selects the listen only mode. The setting of the remaining address switches is then irrelevant.
(54)	Internal Standard Frequency Adjustment	An aperture provides access for frequency adjustment of the internal standard.

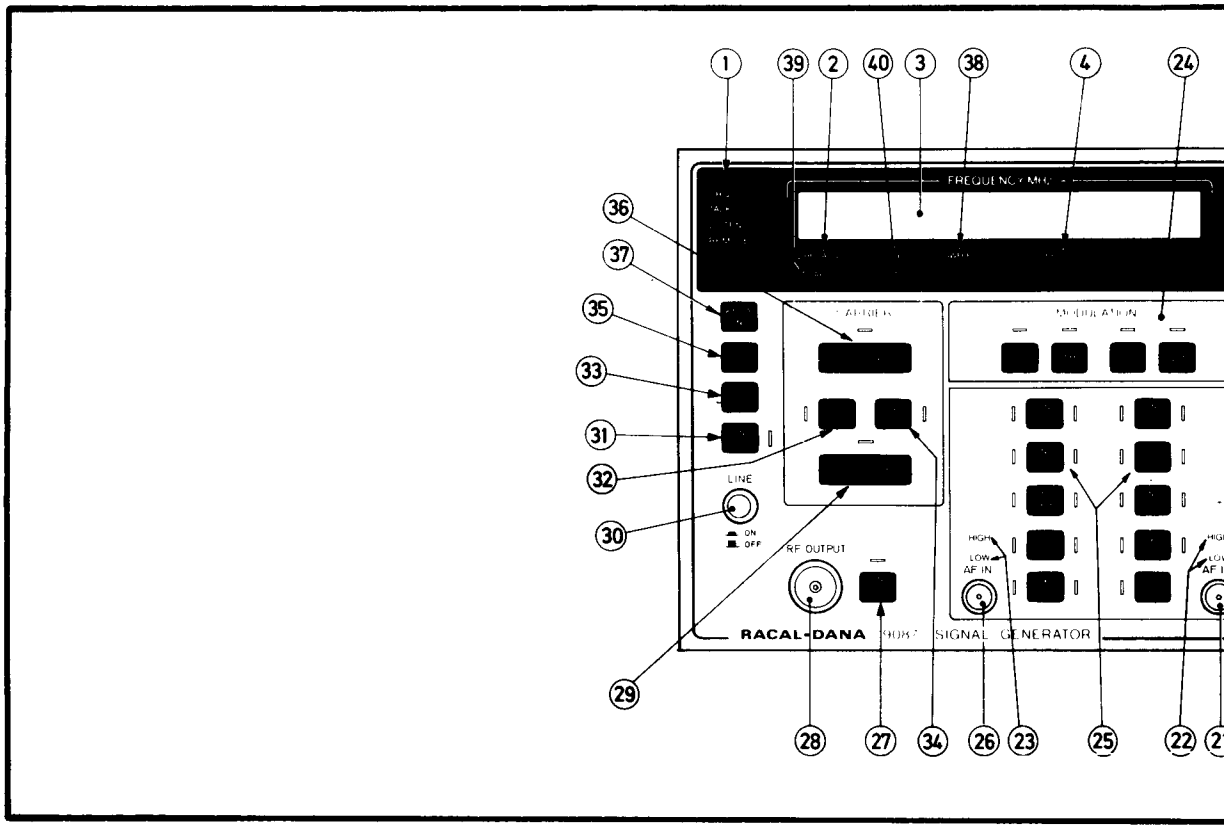
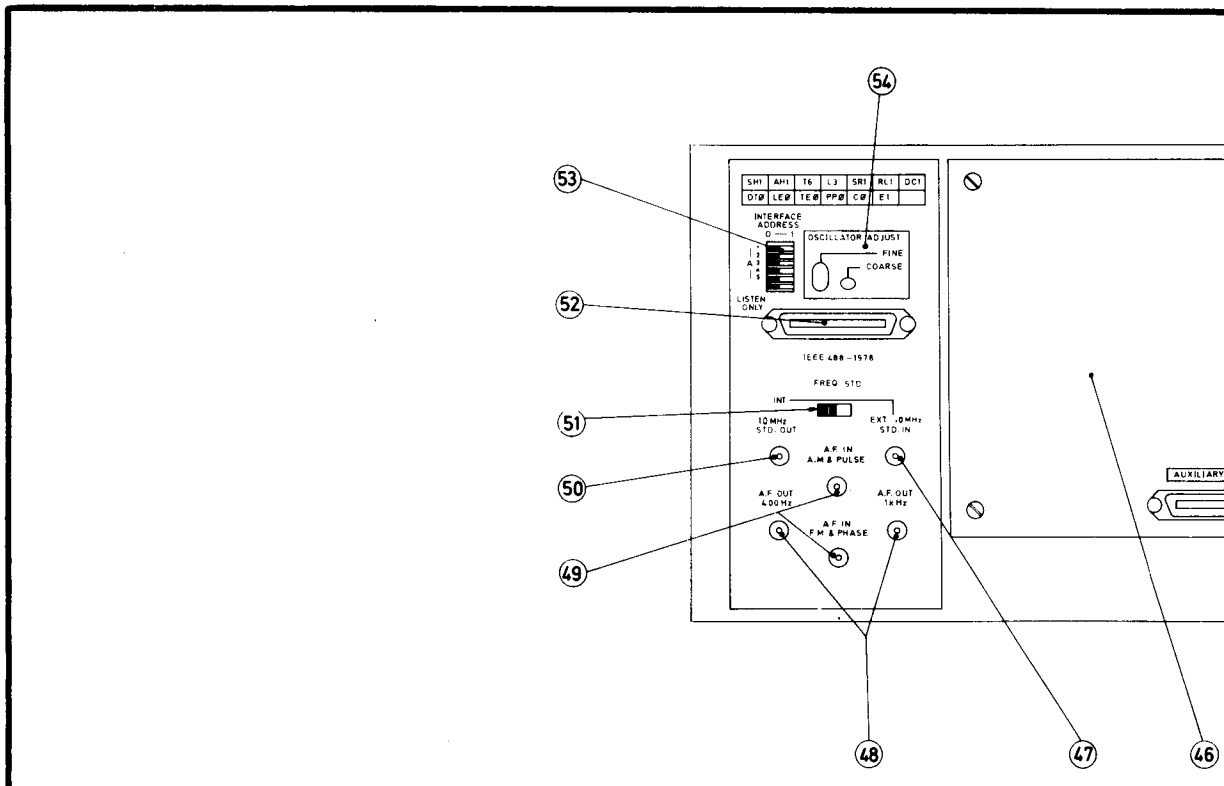

1
39
2
40
3
38
4
24
36
37
35
33
31
32
30
29
28
27
34
26
23
25
22
LINE
ON
OFF
RF OUTPUT
HIGH
LOW
AF IN
RACAL-DANA
SIGNAL GENERATOR

Fig. 4.


54
53
52
51
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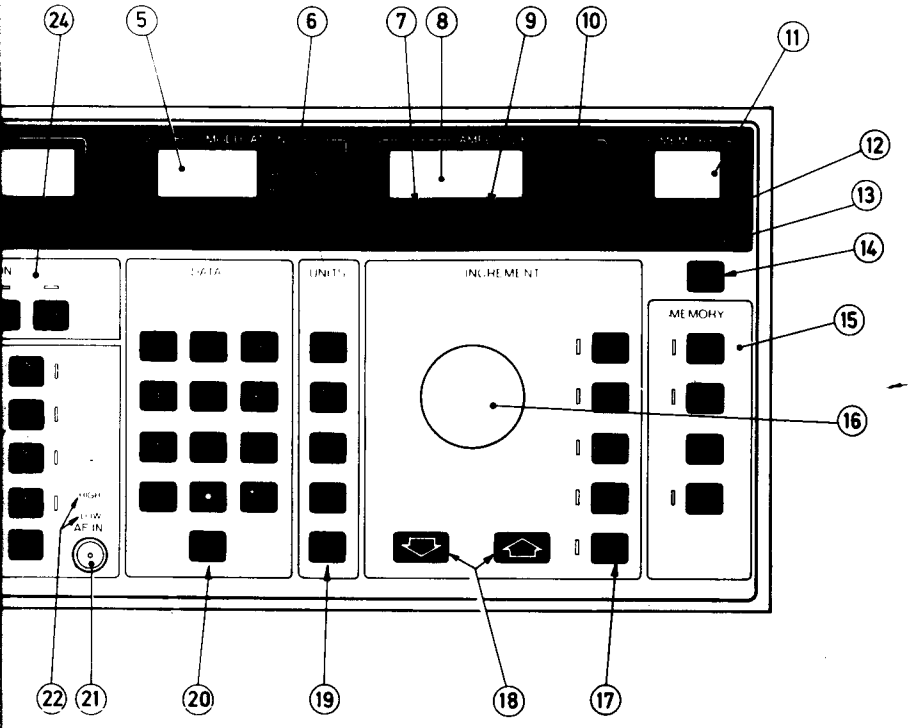
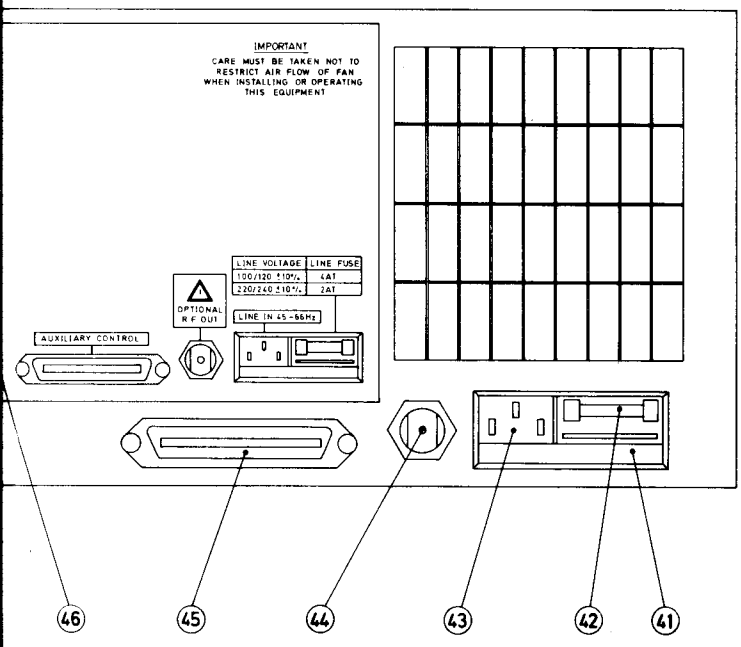
48
47
46
INTERFACE ADDRESS
OSCILLATOR ADJUST
FINE
COARSE
LISTEN ONLY
IEEE 488-1978
FREQ STD
INT
10MHz STD. OUT
A.F. IN A.M & PULSE
A.F. OUT 400Hz
A.F. OUT 1kHz
A.F. IN FM & PHASE
AUXILIARY

Fig. 4.2



ig. 4.1 Front Panel



g. 4.2 Rear Panel

4.3 SWITCHING ON

4.3.1 Connect the instrument to the AC supply and set the LINE switch to ON. All the front-panel LEDs will light for two seconds, after which the address set on the GPIB interface is displayed for 2 seconds. Error code 80 will be generated for a few minutes until the reference generator is in-lock. Once this sequence is complete, the instrument is ready for use, but time must be allowed for the frequency standard to reach operating temperature if the specified accuracy is required. The time required for the internal frequency standard is 6 minutes, for option 04A, and 20 minutes for options 04B and 04L5.

4.3.2 On switching-on, checks are made of the microprocessor's random-access memory (RAM) and the read-only memory (ROM). If errors are found, error code 01 or 02 will be generated, and the number of the faulty memory IC will be displayed. Further operation of the instrument is inhibited until the fault is corrected.

4.3.3 During the switching-on sequence, the front panel is automatically checked for stuck keys. If a fault is found, error code 03 is generated and the code number of the faulty key is displayed.

4.3.4 A check is also made of the non-volatile memory. If an error is found, error code 51 will be generated, and the number of the faulty memory IC will be displayed. Operation of the instrument is not inhibited when this fault is present, but data recalled from memory should be checked before use.

4.3.5 On switching-on, the instrument will be set to the same settings that were in use when the AC power was last switched off.

4.4 SIMPLIFIED OPERATING PROCEDURE

4.4.1 The basic functions of the signal generator are shown in Fig. 4.3. The procedure for changing displayed values is shown in Fig. 4.4.

4.5 OPERATING INSTRUCTIONS

4.5.1 Detailed operating instructions are given in paragraphs 4.5.2 to 4.5.23.

	FUNCTION	DATA				UNITS
FREQUENCY	FREQUENCY	1	9	.	3	MHz
AM DEPTH	AM		8	0		%
FM DEVIATION	FM		7	5		kHz
PHASE MODULATION	ΦM			4		Rads
AMPLITUDE	AMPLITUDE	+/-	1	2	6	dB

The parameters in the examples above are selected by value and follow the Function - Data - Units format.

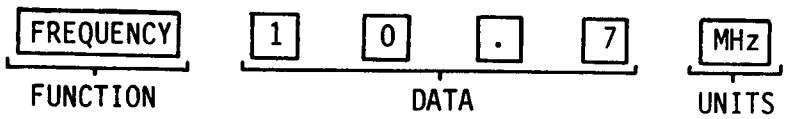
Modulation source. There are two internal modulation signals (400 Hz or 1 kHz). Either of these may be selected, or an external signal AC or DC coupled via the front panel connectors.

Fig. 4.3 Basic Signal Generator Functions

The values of all parameters are selectable in one or more of four different ways.

(1) Data entry via keyboard.
(2) Increment via Step-up/Step-down keys or auxiliary inputs.
(3) Spinwheel increment
(4) GPIB programming.

1. Data entry takes the form Function - Data - Units, e.g.



2. Function values can be changed in selectable steps by pressing the ⇧ step up or ⇩ step down keys or by using external switches connected to the AUXILIARY CONTROL SOCKET on the rear panel.

3. Values can also be changed in selectable steps by rotating the spinwheel in either direction.

4. Complete instrument operation and parameter setting can be achieved by using a GPIB controller. The instrument accepts simple instructions in the form FQ 125 MZ (frequency of 125 MHz).

Fig. 4.4 Changing Values

Frequency

4.5.2

Description This instruction describes how to set the RF signal frequency.

Operating Characteristics:
Range: 10 kHz to 1300.000 000 MHz
Resolution: 1 Hz

Procedure Select FREQUENCY, data and units

Example:

Set RF signal to 232.71 MHz			
	Function	Data	Units
LOCAL (Keystrokes)	FREQUENCY	2 3 2 . 7 1	MHz
GPIB (program codes)	FQ Function	2 3 2 . 7 1 Data	MZ Units

Keys and Program Codes

GPIB

Keys	Codes
FREQUENCY	FQ
GHz	GZ
MHz	MZ
kHz	KZ
Hz	HZ

Associated Error Codes

Code	Reason
10	Frequency entered greater than 1.3 GHz
11	Frequency entered less than 10 kHz
40	Sequence error

Indications When the FREQUENCY key is pressed the indicator above the key lights. This shows that data entries will be directed to the frequency system.

The digits of the selected frequency enter the display as the keys are pressed. Up to 10 digits and a decimal point may be entered.

When the units key is pressed the display is realigned to show the frequency entered in MHz, with 1 Hz resolution, regardless of the units in which entry was made.

Leading zeros are blanked.

Comments

Up to the point where the units key is pressed, the entry can be corrected using the BACKSPACE key, or by reselecting FREQUENCY and starting the entry again.

The output frequency changes to the value entered when the units key is pressed.

The output frequency will be set to 1.3 GHz when error code 10 is generated and 10 kHz when error code 11 is generated. The true output frequency, not the value entered, will be displayed.

When the FREQUENCY indicator is lit, the frequency displayed can be changed using the increment controls.

As an alternative to the use of the units code, the frequency set via the GPIB can be expressed in exponential form, e.g. FQ1376.2E+03 will set a frequency of 1.3762 MHz. Frequency data will be assumed to be in Hz for entries made in the exponential format.

The code FQ sent without data will select frequency as the primary function.

Related Instructions

Frequency, Relative
Increment,
Step Size, Operator-Set
Frequency, Sweep

Frequency, Relative

4.5.3

Description

This instruction describes how to set the output frequency and display it relative to a chosen reference frequency.
Operating Characteristics:
Frequency Offset Range: 1 Hz to 1299.990 000 MHz

Procedure

Set the required reference frequency
Press [REL] (LED on and RELATIVE indicator below frequency display lit).
Set the displayed offset such that
Required output frequency = Reference frequency + Displayed frequency offset.
To return to the normal display mode, ensure that the FREQUENCY key indicator is lit and then press either [REL] or [FREQUENCY]

Example

Set a reference frequency of 11.7 MHz. Set the output frequency to have an offset of 75 kHz below the reference and display the offset. (Output frequency is 11.625 MHz).

	Function	Data				Units
LOCAL (keystrokes)	[FREQUENCY]	[1]	[1]	[.]	[7]	[MHz]
	[REL]	[±]	[7]	[5]		[kHz]
GPIB (program codes)	FQ	11.7				MZ
	FR	-75				KZ
	Function	Data				Units

Keys and Program Codes

GPIB

Keys	Codes
FREQUENCY	FQ
FREQUENCY and REL	FR
GHz	GZ
MHz	MZ
kHz	KZ
Hz	Hz

Associated Error Codes

Code	Reason
12	Reference frequency and frequency offset entered require an output frequency greater than 1.3 GHz
13	Reference frequency and frequency offset entered require an output frequency less than 10 kHz
40	Sequence error.

Indications

When the FREQUENCY key is pressed, the indicator above the key lights. This shows that data entries will be directed to the frequency system.

When the reference frequency has been set, this value, in MHz, will be shown in the frequency display.

When the REL key is pressed, the key indicator will light. A RELATIVE legend below the frequency display will be illuminated and the frequency display will show the last frequency offset entered.

The digits of the new frequency offset enter the display as the keys are pressed. Up to 10 digits and a decimal point may be entered.

Comments

When the REL key is pressed, the output frequency will change to a value determined by the last frequency offset entered.

Up to the point when the units key is pressed, the entry can be corrected using the BACKSPACE key.

The frequency offset entered is set, and the output frequency changes, when the units key is pressed.

The ± key is only required when entering negative offsets. It can be used at any point during the data entry.

The sign of the displayed offset can be changed by pressing ± and any frequency units key.

If any function key other than FREQUENCY is operated, the relative mode for frequency is maintained. The REL key indicator will be extinguished, but the RELATIVE indicator below the frequency display will remain lit.

When the FREQUENCY and REL key indicators are lit, the displayed frequency offset can be changed using the increment controls.

The output frequency will be set to 1.3 GHz when error code 12 is generated and 10 kHz when error code 13 is generated. The actual offset, not the value entered, will be displayed.

GPIB

As an alternative to the use of the units code, the offset can be expressed in exponential form, e.g. FR-12.5E+03 will set a negative frequency offset of 12.5 kHz. Frequency data will be assumed to be in Hz for entries made in the exponential format.

The code FR sent without data will put the instrument into the relative frequency mode, using the last frequency offset entered.

Related Instructions

Frequency
Increment
Step Size, Operator-Set

Frequency, Sweep

4.5.4

Description

This instruction describes how to set up and use the frequency sweep facility.

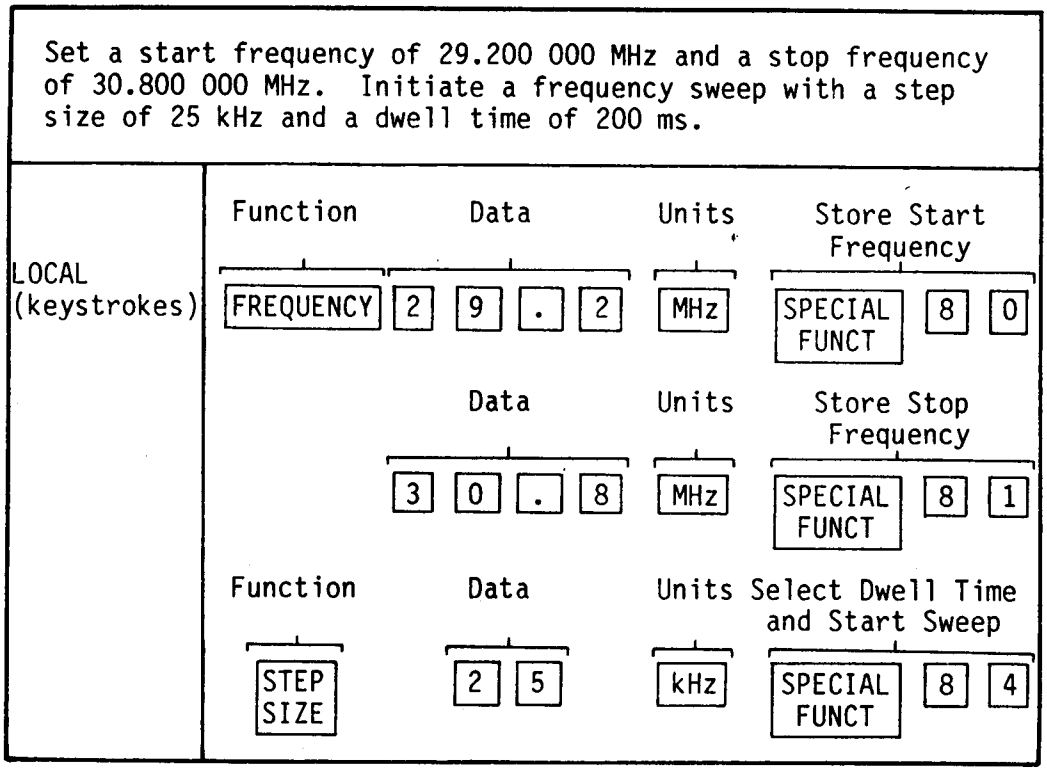
Operating characteristics:
- Start frequency: 10.000 kHz to 1299.999 999 MHz
- Stop frequency : 10.001 kHz to 1300.000 000 MHz
- Increasing frequency sweep only is permitted.
- Frequency step size: 1 Hz to 1299.990.MHz
- Dwell time: 2 ms : Special Function 82
  20 ms : Special Function 83
  200 ms : Special Function 84
  1 s : Special Function 85

Procedure

Set start frequency
Set stop frequency
Set step size
Select dwell time and start sweep
To stop the sweep, press any key or operate the spinwheel.

Example

Set a start frequency of 29.200 000 MHz and a stop frequency of 30.800 000 MHz. Initiate a frequency sweep with a step size of 25 kHz and a dwell time of 200 ms.



GPIB (program codes)	FQ Function	29.2 Data	MZ Units	DG 8Ø Store Start Frequency
		3Ø.8 Data	MZ Units	DG 81 Store Stop Frequency
	FS Function	25 Data	KZ Units	DG 84 Select Dwell Time and start sweep

Keys and Program Codes

GPIB

Keys	Codes
FREQUENCY	FQ
GHz	GZ
MHz	MZ
kHz	KZ
Hz	HZ
SPECIAL FUNCT	DG

Associated Error Codes

Code	Reason
40	Sequence error
45	Attempt made to start sweep with step size of zero

Indications

When the sweep is operating, a SWEEP legend appears below the frequency display.

The frequency display shows the output frequency throughout.

Comments

The start and stop frequencies can be displayed, whether the sweep is operating or not, using special functions 86 and 87. A SWEEP START or SWEEP STOP legend will appear below the frequency display. If the start frequency stored is greater than the stop frequency stored, the values will be exchanged when the sweep is started.

The step size used for the sweep is the operator-set step size for frequency increments. Any previously entered step size will be overwritten.

If the sweep is interrupted, it will restart from the start frequency.

Related Instructions

Frequency
Step Size, Operator-Set

Amplitude

4.5.5

Description

This instruction describes how to set RF signal amplitude.

Operating Characteristics:
Range: +19 dBm to -140 dBm (2 V - 22.4 nV) into 50 Ω.
Resolution: 0.1 dBm

Residual Signal Level:
With the RF output off, the residual signal output will be at least 150 dB/Hz below the carrier level set.

Carrier Level Settling Time:
The carrier level is reestablished 400 µs after switching the RF on.

Procedure

Select AMPLITUDE, data, and units.

To turn the RF output on, press output [ON OFF] (LED on)

To turn the RF output off, press output [ON OFF] (LED off)

Example

Set RF signal amplitude to -12.7 dBm or 51.8 mV

	Function	Data	Units
LOCAL (keystrokes)	AMPLITUDE	+/- 1 2 . 7	dB
or	AMPLITUDE	5 1 . 8	mV

GPIB (program codes)

AP -12.7 DB (Function: AP; Data: -12.7; Units: DB)

OR

AP 51.8 MV (Function: AP; Data: 51.8; Units: MV)

Keys and Program Codes

GPIB

Keys	Codes
AMPLITUDE	AP
V	VO
mV	MV
µV	UV
nV	NV
dB	DB
RF OUTPUT ON	OP1
RF OUTPUT OFF	OPØ

Associated Error Codes

Code	Reason
15	Amplitude input exceeds +19 dBm or 2.0 V
16	Amplitude input less than -140 dBm or 22.4 nV
40	Sequence error

Indications

When the AMPLITUDE key is pressed the indicator above the key lights. This shows that data entries will be directed to the amplitude system.

The digits of the selected amplitude enter the display as the keys are pressed. Up to four digits and a decimal point can be entered. The units indicator lights when the units key is pressed.
When the units key is pressed, the display shows up to four digits, with resolution of 0.1 dB, for amplitudes entered in dBm or up to three digits, with floating decimal point, for amplitudes entered in voltage units.

Up to the point where the units key is pressed, the entry can be corrected using the BACKSPACE key, or by reselecting AMPLITUDE and starting the entry again.

The output amplitude changes to the value entered when the units key is pressed.

The output amplitude will be set to +19 dB (2 V) when error code 15 is generated and -140 dBm (22.4 nV) when error code 16 is generated. The true amplitude, not the value entered, will be displayed.

When the AMPLITUDE indicator is lit, the amplitude displayed can be changed using the increment controls.

Comments

The display units may be changed from 'volts' to 'dB' by pressing the dB key. Similarly, pressing any 'VOLTS' key will change the display mode to 'VOLTS' mode from 'dB' mode.

As an alternative to units code, the value may be expressed in exponential form, e.g. AP100E-03 (100 mV). Amplitude data will be assumed to be in volts. Units conversion may be achieved via GPIB by transmitting no data with the required units, e.g., APUV. This will not change the actual output amplitude.

Related Instructions

Amplitude, Relative
Increment
Step Size, Operator-Set.

Amplitude, Relative

4.5.6

Description

This instruction describes how to set the output amplitude to have an operator-selectable offset from a chosen reference amplitude.

Operating Characteristics:
Amplitude Offset Range: 0.1 dB to 159 dB
0.1 nV to 1.99 V

Procedure

Set the required reference amplitude
Press [REL] (LED on and RELATIVE indicator below amplitude display lit).
Set the displayed offset such that
Required output amplitude = Reference amplitude +
Displayed amplitude offset.

To return to the normal display mode, ensure that the AMPLITUDE key indicator is lit and then press either [REL] or [AMPLITUDE]

Example 1

Set a reference amplitude of 1 V. Set the output amplitude to have an offset of 0.1 V below the reference and display the offset. (Output amplitude is 900 mV).

	Function	Data	Units
LOCAL (keystrokes)	[AMPLITUDE]	[1]	[V]
	[REL]	[±] [.] [1]	[V]
GPIB (program codes)	AP	1	VO
	AR	- . 1	VO
	Function	Data	Units

Example 2

Set a reference amplitude of 1 µV. Set the output amplitude to be 30 dB above the reference level. (Output amplitude is +30 dBµV.)

	Function	Data	Units
LOCAL (keystrokes)	AMPLITUDE REL	1 3 0	µV dB
GPIB (program codes)	AP AR Function	1 3Ø Data	UV DB Units

Keys and Program Codes

GPIB

Keys	Codes
AMPLITUDE	AP
AMPLITUDE and REL	AR
V	VO
mV	MV
µV	UV
nV	NV
dB	DB

Associated Error Codes

Code	Reason
17	Reference amplitude and amplitude offset entered demand an output amplitude greater than +19 dBm (2 V)
18	Reference amplitude and amplitude offset entered demand an output amplitude less than -140 dBm (22.4 nV)
40	Sequence error

Indications

When the AMPLITUDE key is pressed, the indicator above the key lights. This shows that data entries will be directed to the amplitude system.

When the reference amplitude has been set, this value, in dB or voltage units, will be shown in the amplitude display.

When the REL key is pressed, the key indicator will light. A RELATIVE legend below the amplitude display will be illuminated, and the amplitude display will show the last amplitude offset entered.

Comments

When the REL key is pressed, the output amplitude will change to a value determined by the last amplitude offset entered.

Up to the point where the units key is pressed, the entry can be corrected using the BACKSPACE key.

The amplitude offset entered is set, and the output amplitude changes, when the units key is pressed.

The offset can be entered in dB relative to a voltage level, or in voltage units relative to a level in dBm.

The ± key is only required when entering negative offsets. It can be used at any point during the data entry.

The reference amplitude and the amplitude offset may be entered in any combination of dB and voltage units.

The sign of the displayed offset can be changed by pressing [±] and the units key corresponding to the displayed value.

If any function key other than [AMPLITUDE] is operated, the relative mode for amplitude is maintained. The REL key indicator will be extinguished, but the RELATIVE indicator below the amplitude display will remain lit.

The output amplitude will be set to +19 dBm (2 V) when error code 17 is generated and -140 dBm (22.4 nV) when error code 18 is generated. The actual offset, not the value entered, will be displayed.

When the AMPLITUDE and REL key indicators are lit, the displayed amplitude offset can be changed using the increment controls.

GPIB

As an alternative to the use of the units code, the offset can be expressed in exponential form, e.g. AR-12E-03 will set a negative amplitude offset of -12 mV. Amplitude data will be assumed to be in volts for entries made in the exponential format.

The code AR sent without data will put the instrument into the relative frequency mode, using the last amplitude offset entered.

Related Instructions

Amplitude
Increment
Step Size, Operator-Set

Modulation, Amplitude

4.5.7

Description

This instruction describes how to set up and use the AM system.

Operating Characteristics:
AM Depth: 0% to 99%
Resolution: 1%
Modulating Frequency:

Carrier Frequency	Internal Source	External Source
1.5 MHz to 1300 MHz	400 Hz or 1 kHz	AC: 20 Hz to 20 kHz (-3dB) DC: DC to 20 kHz (-3dB)
400 kHz to 1.5 MHz	400 Hz or 1 kHz	AC: 20 Hz to 5 kHz (-3dB) DC: DC to 5 kHz (-3dB)
10 kHz to 400 kHz	400 Hz or 1 kHz	AC: 20 Hz to 100 Hz DC: DC to 100 Hz

Procedure

Select AM, data and %
Select Modulating frequency or external source.

To turn modulation on, press AM [ON OFF] ■ (LED on)

To turn modulation off, press AM [ON OFF] □ (LED off)

Example

Set AM, 75% depth, 1 kHz frequency from internal source and switch modulation on.

	Function	Data	Units	Source	ON
LOCAL (keystrokes)	[AM]	[7] [5]	[%]	[INT 1kHz]	[ON OFF]
GPIB (program codes)	AM Function	75 Data	% or PC Units	MA3 Source	MA1 ON

Keys and Program Codes

GPIB

Keys	Codes
AM	AM
%	% or PC
OFF	MAØ
ON	MA1
400 Hz INT	MA2
1 kHz INT	MA3
EXT AC	MA4
EXT DC	MA5

Associated Error Codes

Code	Reason
24	AM depth entry excessive
25	AM depth excessive for output amplitude
32	External modulating signal input level too low
33	External modulating signal input level too high
40	Sequence error

Indications

When the AM key is pressed the indicator above the key lights. This shows that data entries will be directed to the AM system.

When the AM key is the last MODULATION key pressed, the modulation depth is shown in the modulation display. Two digits are displayed.

The CAL? indicator to the right of the modulation display lights if AM is enabled with

(a) EXT DC selected
(b) EXT AC selected with a carrier frequency below 1.5 MHz
(c) a carrier frequency below 150 kHz.

When AM is selected as the form of modulation given by the AM/Pulse system, the status of the system is shown by the indicators to the right of the control keys.

Comments

Up to the point where the % key is pressed, the entry can be corrected by means of the BACKSPACE key.

The resolution for AM depth is 1%. Entries made with greater resolution will be rounded to the nearest 1% when the % key is pressed.

Whenever AM is selected as the form of modulation to be given by the AM/PULSE modulation system, the control keys remain functional when the AM primary function key indicator is not lit.

When AM is deselected, the settings of the system control keys for AM are stored. The stored values will be recalled when AM is reselected.

In addition to the use of the units code the modulation depth set via the GPIB can be expressed in exponential form, e.g., AM5.7E+01 will set a modulation depth of 57%. Amplitude modulation data will be assumed to be in %.

Related Instructions

Modulation, External Source
Modulation, Mixed
Increment

Modulation, Pulse

4.5.8

Description

This instruction describes how to set up and use the pulse modulation system.

Operating Characteristics (maximum OFF time of 25 ms)

ON/OFF Ratio:
>50 dB for carrier frequency from 10 MHz to 750 MHz
>35 dB for carrier frequency from 750 MHz to 1300 MHz.

Rise and Fall Time:
<40 ns

Modulating Frequency:

Carrier Frequency	Internal Source	External Source
10 MHz to 1300 MHz	400 Hz and 1 kHz	AC: 20 Hz to 2.5 MHz DC: DC to 2.5 MHz

Procedure

Select PULSE

Select internal modulating frequency or external source.

To turn modulation on, press Pulse ON/OFF (LED on)

To turn modulation off, press Pulse ON/OFF (LED off)

Example

Enable pulse modulation, external source, DC coupled and switch modulation on.

	Function	Source	ON
LOCAL (keystrokes)	PULSE	EXT DC	ON OFF
GPIB (program codes)	PM Function	MP5 Source	MP1 ON

Keys and Program Codes

Keys	Codes
PULSE	PM
OFF	MPØ
ON	MP1
400 Hz INT	MP2
1 kHz INT	MP3
EXT AC	MP4
EXT DC	MP5

Associated Error Codes

Code	Reason
32	External modulating signal input too low
33	External modulating signal input too high
40	Sequence error
42	Data input attempted with PULSE selected

Indications

When the PULSE key is pressed, the indicator above the key lights.

When the PULSE key is the last MODULATION key pressed, the modulation display is blanked. A PULSE indicator to the right of the display lights.

When PULSE is selected as the form of modulation given by the AM/Pulse system, the status of the system is shown by the indicators to the left of the control keys.

If pulse modulation is enabled with a carrier frequency below 10 MHz, the CAL? indicator will light.

Comments

No data entry may be made with PULSE selected.

Whenever pulse modulation is selected as the form of modulation given by the AM/PULSE modulation system, the control keys remain functional when the pulse modulation primary function key indicator is not lit.

When PULSE is deselected, the settings of the system control keys for pulse modulation are stored. The stored values will be recalled when PULSE is reselected.

Related Instructions

Modulation, External Source
Modulation, Mixed.

Modulation, Frequency

4.5.9

Description

This instruction describes how to set up and use the FM system.

Operating Characteristics:
- Peak Deviation: 0 kHz to 999 kHz (dependent on frequency, see Section 1)
- Maximum Resolution: 10 Hz
- Modulating Frequency:

Carrier Frequency	Internal Source	External Source
10 kHz to 1300 MHz	400 Hz or 1 kHz	AC: 20 Hz to 100 kHz (-3dB) DC: DC to 100 kHz (-3dB)

Procedure

Select FM, data and units

Select modulating frequency or external source

To turn modulation on, press FM  (LED on)

To turn modulation off, press FM  (LED off)

Example

Set FM peak deviation to 12.5 kHz, 400 Hz internal modulation source and switch modulation on

	Function	Data	Units	Source	ON
LOCAL (keytrokes)	FM	1 2 . 5	kHz	INT 400 Hz	ON OFF
GPIB (program codes)	FM	12.5	KZ	MF2	MF1
	Function	Data	Units	Source	ON

Keys and Program Codes

GPIB

Keys	Codes
FM	FM
MHz	MZ
kHz	KZ
Hz	HZ
OFF	MFØ
ON	MF1
400 Hz INT	MF2
1 kHz INT	MF3
EXT AC	MF4
EXT DC	MF5

Associated Error Codes

Code	Reason
20	Frequency deviation set excessive for carrier frequency in use.
21	Frequency deviation entry excessive for frequency range in use
30	External modulating signal input too low
31	External modulating signal input too high
40	Sequence error

Indications

When the FM key is pressed, the indicator above the key lights. This shows that data entries will be directed to the FM system.

When the FM key is the last MODULATION key pressed, the peak deviation is shown in the modulation display. Up to three digits and a decimal point are displayed. Excess digits are ignored. The deviation is displayed in kHz, with the greatest possible resolution, regardless of the units of entry.

When FM is selected as the form of modulation given by the FM/ØM system, the status of the system is shown by the indicators to the left of the control keys.

When FM is used with EXT DC selected, the CAL? indicator to the right of the modulation display will light.

Comments

Up to the point where the units key is pressed, the entry can be corrected using the BACKSPACE key.

Entries made with resolution greater than 10 Hz will be rounded and displayed to the nearest 10 Hz.

Whenever FM is selected as the form of modulation given by the FM/ØM system, the control keys remain functional when the FM primary function key indicator is not lit.

When FM is deselected, the settings of the system control keys for FM are stored. The stored values will be recalled when FM is reselected.

When the FM indicator is lit, the peak deviation displayed can be changed using the increment controls.

In addition to the use of the units code, the peak deviation set via the GPIB can be expressed in exponential form, e.g., FM 12.5E+03 will set a peak deviation of 12.5 kHz. Frequency modulation data will be assumed to be in Hz.

Related Instructions

Modulation, External Source
Modulation, Mixed
Increment

Modulation, Phase

4.5.10

Description

This instruction describes how to set up and use the phase modulation system.

Operating Characteristics:

Peak-Phase Deviation:

Carrier Frequency	Maximum Peak-Phase Deviation
10 kHz to 60 kHz	As given by $\frac{\text{Carrier frequency} - 10^4}{\text{Modulating frequency}}$ radians
60 kHz to 130 MHz	5 radians

Resolution: 0.01 radian
Modulating Frequency: 400 Hz or 1 kHz from internal source
20 Hz to 10 kHz (-3 dB) from external source

Procedure

Select ØM, data and Rads

Select modulating frequency or external source.

To turn modulation on, press Phase Modulation [ON OFF] ■ (LED on)

To turn modulation off, press Phase Modulation [ON OFF] □ (LED off)

Example

Set Phase Modulation, peak deviation to 1.57 radians, external source, AC coupled, and switch modulation on.

	Function	Data	Units	Source	ON
LOCAL (keystrokes)	[ØM]	[1] [.] [5] [7]	[Rads]	[EXT AC]	[ON OFF]
GPIB (program codes)	HM	1.57	RD	MH4	MH1
	Function	Data	Units	Source	ON

Keys and Program Codes

GPIB

Keys	Codes
ØM	HM
Rads	RD
OFF	MHØ
ON	MH1
400 Hz INT	MH2
1 kHz INT	MH3
EXT AC	MH4

Associated Error Codes

Code	Reason
22	Peak phase deviation entered excessive
23	Peak phase deviation excessive for carrier frequency
30	External modulating signal input too low
31	External modulating signal input too high
40	Sequence error
43	External modulating signal input with DC coupling not permitted

Indications

When the ØM key is pressed, the indicator above the key lights. This shows that data entries will be directed to the phase modulation system.

When the ØM key is the last MODULATION key pressed, the peak phase deviation is shown in the modulation display. Three digits and a decimal point are displayed.

When phase modulation is selected as the form of modulation given by the FM/ØM system, the status of the system is shown by the indicators to the right of the control keys.

Comments

Up to the point where the RADS key is pressed, the entry can be corrected by means of the BACKSPACE key.

The resolution for peak-phase deviation is 0.01 radian.

Whenever phase modulation is selected as the form of modulation given by the FM/ØM system, the control keys remain functional when the ØM primary function key indicator is not lit.

When phase modulation is deselected, the settings of the system control keys for phase modulation are stored. The stored values will be recalled when phase modulation is reselected.

If phase modulation is enabled with a carrier frequency less than 60 kHz, the CAL? indicator to the right of the modulation display lights to warn that the calibration of the display is not guaranteed.

When the ØM indicator is lit, the peak phase deviation displayed can be changed using the increment controls.

In addition to the use of the units code, the peak-phase deviation set via the GPIB can be expressed in exponential form, e.g., HM3.5E-01 will set a peak-phase deviation of 0.35 radians. Phase modulation data will be assumed to be in radians.

Related Instructions

Modulation, External Source
Modulation, Mixed
Increment

Modulation, Mixed

4.5.11

Description

This instruction describes how to operate the instrument with more than one modulation system active.

Operating Characteristics:

Possible Modulation Combinations:
- AM and FM
- AM and ΦM
- Pulse and FM
- Pulse and ΦM

Procedure

Set the required modulation parameters for the forms of modulation to be used, as instructed in the individual modulation instructions.

Enable and disable the modulation systems using the appropriate ON/OFF key.

To change the form of modulation provided by a system, press the primary function key for the required modulation. The modulation parameters last used with that form of modulation will be recalled.

Example

Change from AM+FM to PULSE+FM, using the previously stored parameters for pulse modulation. Enable pulse modulation.

LOCAL (keystrokes)	System Changeover: [PULSE]	Enable: [ON] [OFF]	Enablement is not required if this is already included in the stored settings
GPIB (program codes)	MP1 — Select Pulse Modulation and Enable	OR	PM — Select Pulse Modulation. Set stored control settings

Indications

The modulation display shows the parameters of the form of modulation selected by the last operation of a modulation primary function key. The form of modulation is shown by the units indicator or PULSE indicator.

The status of the selected form of modulation for each system is shown by the indicators beside the control keys.

Related Instructions

Modulation, Amplitude
Modulation, Pulse
Modulation, Frequency
Modulation, Phase
Modulation, External Source

Modulation, External Source

4.5.12

Description

This instruction describes how to connect and set the level of an external modulating signal source.

Operating Characteristics:

Input Socket: Separate BNC sockets are provided for the AM/PULSE and FM/ØM systems.

Input Impedance: 16 kΩ for PULSE
600 Ω for AM, FM and ØM

Input Level:

	AC	DC
AM	0.56 V to 5.6 V peak-to-peak	1.414 V peak
PULSE	>3.0 V peak-to-peak	ON = >1.7 V OFF = <0.9 V
FM	0.56 V to 5.6 V peak-to-peak	1.414 V peak
ØM	0.56 V to 5.6 V peak-to-peak	DC coupling not permitted

Procedure

Connect external source to the appropriate input socket.

Switch on source.

Select the external modulating source, with AC or DC coupling, as required, using the appropriate modulation system control key.

Adjust the source level.

NOTE: For AC coupling with AM, FM or ØM, the level should be adjusted until the HIGH and LOW indicators adjacent to the AF input socket are both extinguished. For all other cases, the level must be set using external measuring equipment.

Related Instructions

Modulation, Amplitude
Modulation, Pulse
Modulation, Frequency
Modulation, Phase
Modulation, Mixed

Increment

4.5.13

Description

This instruction describes how to step a displayed value up or down by a preselected amount using the step keys, auxiliary control inputs, or the spinwheel.

Operating Characteristics:

Controllable Parameters: Frequency
Frequency offset
Amplitude
Amplitude offset
AM depth
FM peak deviation
ΦM peak deviation
Memory location (in recall mode only)

Parameter Selection: By means of the primary function key or RECALL key relating to the display to be changed.

Step Size Selection: By means of the COARSE, MEDIUM and FINE sensitivity keys or the STEP key.

NOTE: The use of the STEP key is permitted for frequency or amplitude only.

Step Sizes Available:

Primary Function	Step Size		
	Coarse	Medium	Fine
Frequency	1 MHz	1 kHz	1 Hz
Amplitude (volts)	Most significant digit	Second digit	Least significant digit
Amplitude (dB)	10 dB	1 dB	0.1 dB
Amplitude Relative (volts)	Most significant digit of reference level	Second digit of reference level	Least significant digit of reference level

AM depth	10 %	5 %	1%
FM peak deviation	Most significant digit	Second digit	Least significant digit
ØM peak deviation	1 rad	0.1 rad	0.01 rad
Memory (recall mode only)	One memory location		

Spinwheel Disablement: The spinwheel, but not the step keys can be disabled by selecting HOLD (LED on). The spinwheel is enabled by selecting HOLD a second time (LED off).

Procedure

Select required function
Display the parameter to be changed
Select COARSE, MEDIUM or FINE to obtain the required step size.
For frequency and amplitude only, the operator-set step size may be enabled by selecting STEP.
Operate the step-up or step-down key, the external step switch, or the spinwheel.

Example 1

Display the frequency offset and change the offset by -2.998 kHz

LOCAL (keystrokes)

Function: FREQUENCY, REL
Step Size 1 kHz: MEDIUM
-3 kHz: ⇩ ⇩ ⇩
Step Size 1 Hz: FINE
+2 Hz: ⇧ ⇧

The spinwheel or external step switches may be used instead of the step keys

GPIB (program codes)

FR — Function
IN3 — Step Size 1 kHz
FD FD FD — -3 kHz
IN2 — Step Size 1 Hz
FU FU — +2 Hz

Example 2

Display the output amplitude and increase the value displayed by the value of the operator selected step			
LOCAL (keystrokes)	Function AMPLITUDE	Step Size STEP	Step Up ⇧
GPIB (program codes)	IN5 Step Size		AU Amplitude Step Up

Keys and Program Codes

Keys	Codes
FREQUENCY and STEP UP	FU
FREQUENCY and STEP DOWN	FD
AMPLITUDE and STEP UP	AU
AMPLITUDE and STEP DOWN	AD
HOLD (Spinwheel enabled)	INØ
HOLD (Spinwheel disabled)	IN1
COARSE	IN2
MEDIUM	IN3
FINE	IN4
STEP	1N5

Associated Error Codes

Code	Reason
40	Sequence error
41	Invalid use of increment controls

Indications

When the required primary-functions key is pressed, the indicator above the key lights. This shows that data entries from the increment controls will vary the value shown in the corresponding display.

The key indicator to the left of the selected sensitivity key lights.

Comments

The spinwheel should be turned clockwise to increase and counter-clockwise to decrease the parameter to be changed.

A succession of steps can also be obtained by pressing and holding the step-up key or the step-down key.

Software debouncing of the external step switches is selected using special function 05 and disabled using special function 06. The debouncing time is 20 ms.

Related Instructions

Frequency
Frequency, Relative
Amplitude
Amplitude, Relative
Modulation, Amplitude
Modulation, Frequency
Modulation, Phase
Step Size, Operator-Set.

Step Size, Operator Set

4.5.14

Description

This instruction describes how to set the operator-selectable step size for use with the increment controls.

Operating Characteristics:

Range and Resolution:

Function	Units	Range	Resolution
Amplitude	Volts	0.1 nV to 1.99 V	1 LSD of displayed value
Amplitude	dB	0.1 dBm to 159 dBm	0.1 dBm
Frequency	Hz	1 Hz to 1299.99 MHz	1 Hz

Procedure

Select AMPLITUDE or FREQUENCY as required, unless already active.

Press [STEP SIZE] ▮ (LED on)

Enter data and units, using keyboard

If no change to the step size is required, press [STEP SIZE] ▯ (LED off) or any primary function key

Example

Set amplitude step size to 1.2 dB or 51.8 mV

	Function	Step Size	Data	Units
LOCAL (keystrokes)	[AMPLITUDE]	[STEP SIZE]	[1] [.] [2]	[dB]
or	[AMPLITUDE]	[STEP SIZE]	[5] [1] [.] [8]	[mV]

GPIB (program codes)	AS	1.2	dB	or	AS	51.8	MV
	Amplitude Step	Data	Units		Amplitude Step	Data	Units

Keys and Program Codes

Keys	Codes
AMPLITUDE and STEP SIZE	AS
FREQUENCY and STEP SIZE	FS
V	VO
mV	MV
µV	UV
nV	NV
dB	DB
GHz	GZ
MHz	MZ
kHz	KZ
Hz	HZ

GPIB

Associated Error Codes

Code	Reason
14	Frequency step size entry excessive
19	Amplitude step size entry excessive
40	Sequence error
41	Invalid use of increment controls

Indications

The key indicator of the primary function selected will light when the key is pressed.

When STEP SIZE is selected the key indicator will light. A STEP SIZE legend below the display corresponding to the selected function will be illuminated. The display will show the last step size entered.

The display will revert to the normal mode, with the STEP SIZE legend and the STEP SIZE key indicator extinguished, if the STEP SIZE key is operated a second time or if any function key is operated.

The display will revert to the normal mode when the units key is released following the entry of a new step size by means of the keyboard.

Comments

Up to the point where the units key is pressed, the entry can be corrected using the BACKSPACE key.

The increment controls cannot be used to change a displayed step size.

GPIB

In addition to the use of the units code, the step size set via the GPIB can be expressed in exponential form,
e.g., AS1.8E-03 will set an amplitude step size of 1.8 mV;
FS25E+03 will set a frequency step of 25 kHz
Data will be assumed to be in volts or Hz.

Related Instructions

Increment
Frequency Sweep

Initialisation

4.5.15

Description

This instruction describes how to initialize the instrument settings.

Operating characteristics: The instrument initialization routine is as follows:

All the front-panel LEDs will be switched on for two seconds, after which the address set on the GPIB is displayed, in binary and decimal form, for two seconds. A check for corruption of the ROM contents is made, followed by a check of the functioning of the non-volatile memory. The instrument is then set to the following state:

Frequency	100 MHz
Relative frequency offset	0 MHz
Frequency step-size	12.5 kHz
Sweep-start frequency	1 MHz
Sweep-stop frequency	1.3 GHz
Amplitude	-30 dBm
Relative amplitude offset	0 dBm
Amplitude step-size	3 dB
Modulation	All forms disabled
AM/Pulse system	AM
FM/ØM system	FM
AM	0%, 400 Hz INT, OFF
Pulse	400 Hz INT, OFF
FM	0 kHz, 400 Hz INT, OFF
ØM	0 rads, 400 Hz INT, OFF
Modulation display	FM
RF Output	ON
Spinwheel	Enabled
Sensitivity	COARSE
Primary function	FREQUENCY
RPPU (if fitted)	Reset

Procedure

Press [INIT]

Keys and Program Codes

GPIB

Keys	Codes
INIT	IP

Associated Error Codes

Code	Reason
02	ROM contents corrupted
51	Functional failure of non-volatile memory.

Comments

No checks of ROM contents or non-volatile memory function are made, nor front-panel LED or GPIB address display performed, on initialization via the GPIB.

Memory, Store

4.5.16

Description

This instruction describes how to store the current front-panel settings of the instrument in a designated location within the instrument's non-volatile memory.

Operating Characteristics:

Available Locations:	Normal 33 Optional 100
Location Address:	Two-digit number
Write Protection:	Write protection of the whole memory, not individual locations, is available as a special function.

Procedure

Press [STORE] (LED on)
Enter the two-digit address of the required location using the numeric keyboard (EXEC key LED flashes)

Press [EXEC] (LED off)

Example

Store current front-panel settings in memory location 07			
LOCAL (keystrokes)	Function STORE	Location 0 7	Store Displayed Pattern EXEC
GPIB (program codes)	MS Function	Ø7 Location	ME Store Displayed Pattern

Keys and Program Codes

GPIB

Keys	Codes
STORE	MS
EXEC	ME

Associated Error Codes

Code	Reason
40	Sequence error
41	Invalid use of spinwheel or increment keys
44	Exponential entry of address not permitted
50	Memory board not fitted
53	Memory location not available.
54	Single digit entered as address
55	Attempted use of MEM EXCH key
56	Store attempted when WRITE PROTECT is set

Indications

The STORE key indicator lights when the key is pressed. This shows that data entries will be directed to the store system.

The digits of the selected memory location will appear in the memory display as they are entered.

The indicator of the EXEC key will flash when the second address digit is entered.

The indicators of the STORE and EXEC keys are extinguished, and the memory display is blanked when storage is complete.

Comments

Up to the point where the EXEC key is pressed, the memory location may be changed by means of the BACKSPACE key, or by reselecting STORE and making the entry again.

The address entered must contain two digits. A leading zero must be entered for locations 00 to 09.

Location 00 is used to store the instrument's status when power is switched off. Under these circumstances, data in this location will be overwritten.

The spinwheel and step keys cannot be used to change a displayed location address.

The primary function, the special functions enabled, and the SRQ mask setting are not stored.

Memory, Recall (Normal)

4.5.17

Description

This instruction describes how to view the contents of the non-volatile memory locations and set the instrument output to the pattern stored in a selected location.

Operating Characteristics:

Available Locations: Normal 33
Optional 100

Location Address: Two-digit number

Display of Stored Pattern: The pattern stored in a selected location can be displayed on the instrument's front panel without change to the output.

Procedure

Press [RECALL] (LED on)

Enter two digit address of the required location using the numeric keyboard (EXEC key LED flashes).

Change address, if required, using keyboard, spinwheel, or step keys.

To set the output to a displayed pattern, press [EXEC] (LED off).

The instrument leaves the recall mode when this is done.

To leave the recall mode without change of output, press any primary function key.

Example

Examine contents of memory locations 02, 07, 08 and 09. Set the pattern stored in location 09	
LOCAL (keystrokes)	Function [RECALL] Location [0] [2] Function [RECALL] Location [0] [7] Location [⇧] Location [⇧] Set Displayed Pattern [EXEC]

GPIB (program codes)	MR Function, Ø2 Location, MR Function, Ø7 Location MR Function, Ø8 Location, MR Function, Ø9 Location, ME Set Display Pattern

Keys and Program Codes

Keys	Codes
RECALL	MR
EXEC	ME

Associated Error Codes

Code	Reason
40	Sequence error
44	Exponential entry of address not permitted
50	Memory board not fitted
52	Recalled location has a checksum error
53	Recalled location not available
54	Single digit entered as address

Indications

The RECALL key indicator lights when the key is pressed. This shows that data entries from the keyboard or increment controls will be directed to the recall system.

The digits of a location address selected using the keyboard will enter the memory display as they are entered.

The indicator of the EXEC key will flash when the second digit is entered, and the display will show the contents of the selected memory location.

The display reverts to showing the actual instrument output, with the memory display blank, when RECALL is selected before entering a new address.

The RECALL key indicator is extinguished and the memory display is blanked when the instrument leaves the recall mode.

Comments

The Memory Recall (Immediate) mode will provide faster operation if it is not necessary to view the contents of a memory location before setting the instrument output.

Related Instructions

Memory, Recall (Immediate)

Memory, Recall (Immediate)

4.5.18

Description

This instruction describes how to set the instrument output to a setting pattern held in the instrument's non-volatile memory.

Operating Characteristics:

Available Locations:	Normal 33 Optional 100
Location Address:	Two-digit number

Procedure

Press ▌[RECALL] (LED on)

Press ▌[EXEC] (LED on)

Enter two digit address, or change an address already displayed, using the keyboard, spinwheel, or step keys.

To leave the recall mode press any primary function key.

Example

Set the instrument output to the patterns held in memory locations 02, 09, 08, 07 and 08 in succession

LOCAL (keystrokes)	Function: [RECALL] [EXEC] — Location: [0] [2] — Location: [0] [9] — Location: [⇩] — Location: [⇩] — Location: [⇧]
GPIB (program codes)	MR ME — Function — Ø2 — Location — Ø9 — Location — Ø8 — Location — Ø7 — Location — Ø8 — Location

Keys and Program Codes

GPIB

Keys	Codes
RECALL	MR
EXEC	ME

Associated Error Codes

Code	Reason
40	Sequence error
44	Exponential entry of address not permitted
50	Memory board not fitted
52	Recalled location has a checksum error
53	Recalled location not available
54	Single digit entered as address
55	Attempted use of MEM EXCH key

Indications

The RECALL key indicator lights when the key is pressed. This shows that data entries from the keyboard or increment controls will be directed to the recall system.

The EXEC key indicator lights when the key is pressed. It remains lit until the instrument leaves the recall mode.

The digits of a location address selected using the keyboard will enter the memory display as they are entered.

The leading digit of the memory display is blanked when the first digit of a subsequent address is entered using the keyboard.

The RECALL and EXEC key indicators are extinguished and the memory display is blanked when the instrument leaves the recall mode.

Comments

To view the contents of a memory location before setting the instrument output, use the Memory Recall (Normal) mode.

Related Instructions

Memory, Recall (Normal)

Memory, Exchange

4.5.19

Description

This instruction describes how to exchange the contents of two locations in the instrument's non-volatile memory.

Procedure

Press ▌RECALL (LED on)

Enter two digits of first location address (EXEC key LED flashes)

Press MEM EXCH

Enter two digits of second location address

Press ▯EXEC (LED off)

Example

Exchange the contents of memory locations 07 and 22										
LOCAL (keystrokes)	Function	RECALL	Location	0	7	Function	MEM EXCH	Location	2	2	Execute	EXEC
GPIB (program codes)		MR		Ø7			MI		22			ME
		Function		Location			Function		Location			Execute

Keys and Program Codes

GPIB

Keys	Codes
RECALL	MR
MEM EXCH	MI
EXEC	ME

Associated Error Codes

Code	Reason
40	Sequence error
41	Invalid use of spin-wheel or step keys
44	Exponential entry of address not permitted
50	Memory board not fitted
52	Recalled location has checksum error
53	Recalled location not available
54	Single digit entered as address
56	Store attempted when WRITE PROTECT is set

Indications

The RECALL key indicator lights when the key is pressed. This shows that data entries made from the keyboard will be directed to the recall system.

The digits of the first location address appear in the memory display as they are entered.

The EXEC key indicator will flash when the second digit is entered, and the display will show the contents of the selected memory location.

The display reverts to showing the actual output of the instrument, with the memory display blanked, when the MEM EXCH key is pressed.

The digits of the second location address appear in the memory display as they are entered.

The display will show the contents of the selected memory location when the second digit is entered.

The RECALL and EXEC key indicators are extinguished, and the display reverts to showing the actual output of the instrument, with the memory display blanked, when the EXEC key is pressed.

Comments

No change to the actual output of the instrument occurs at any time during the memory exchange procedure.

Since the memory exchange procedure involves writing to the memory, it cannot be performed when WRITE PROTECT is set.

Related Instructions

Special Functions

Standby

4.5.20

Description

This instruction provides information regarding the standby mode.

Operating Characteristics:

Circuits Active in Standby Mode: The internal frequency standard, the microprocessor system, and the battery charging system remain active.

Automatic Entry to Standby Mode: The instrument is automatically switched to standby in the event of overheating.

Procedure

To switch to standby press STAND BY ▮ (LED on)

To revert to normal mode press STAND BY ▯ (LED off)

Keys and Program Codes

GPIB

Keys	Codes
STANDBY (on)	GS1
STANDBY (off)	GSØ

Associated Error Codes

Code	Reason
73	GPIB command interpreted while in standby mode
99	Overtemperature error

Indications

The STANDBY key indicator lights when the key is pressed to switch to standby.

The STANDBY key indicator flashes and SRQ (if enabled) is generated when the instrument is switched to standby following an overtemperature condition.

The BATTERY LOW indicator will light if a full battery charging cycle is in progress.

Apart from the above, all front panel displays and indicators are blanked.

Special Functions

4.5.21

Description This instruction describes how to call and cancel the instrument's special functions.

Procedure Press [SPECIAL FUNCT]

Enter the required special function number.

Special functions marked * are selected automatically on switching-on.

Special functions marked ** are cancelled by the operation of any primary function key or the entry of fresh data.

Special function 20 is cancelled by operating the spinwheel.

Keys and Program Codes

GPIB

Keys	Codes
SPECIAL FUNCT	DG

Associated Error Codes

Code	Reason
40	Sequence error
44	Exponential entry of special function number not permitted
47	Invalid special function number entered

Indications As the special function sequence is entered, the displays will blank and the digits entered will appear in the amplitude display.

For special functions 20, 21, 22, 23, 40, 45, 82, 83, 84, 85, 86 and 87 the special function number appears in the amplitude display while the function is active.

For special functions 71 and 76 the special function number appears in the amplitude display while the check is being carried out. If an error is found, a code number indicating the location of the fault appears in the frequency display and an error code is generated.

Comments The following special functions are available.

Function Number	Function
01	Disable front-panel annunciator
02	Select clunker as annunciator
03	Select beeper as annunciator
05*	External step-switch lines debounced
06	External step-switch lines not debounced
07*	Display out-of-lock error if present
08	Inhibit out-of-lock error display
20	Display code of key held pressed (see Note 3)
21**	Display options code (see Note 1)
22**	Display software revision number
23**	Display special functions selected (see Note 2)
31**	Turn on all displays (LED check)
40**	Display GPIB address. (The test pattern is displayed if set to listen only)
41*	Displays updated at the end of each command received via the GPIB
42	Displays not updated when in remote control
43	Displays updated for each byte received via the GPIB
44	Generate SRQ immediately if bit 7 of the SRQ mask is set
45**	Display the SRQ mask setting
50	Trigger RPPU warning device
51	Reset RPPU warning device
70	Initiate charge cycle for non-volatile memory battery. (The cycle is terminated automatically after approximately 14 hours, or when the instrument is switched off).
71	Check functioning of non-volatile memory
72	Set all memory locations to current instrument settings
73	Remove WRITE PROTECT
74	Set WRITE PROTECT
76	Check for corruption of non-volatile memory data
80	Take present output frequency as sweep-start frequency
81	Take present output frequency as sweep-stop frequency
82**	Sweep-dwell time approximately 2 ms
83**	Sweep-dwell time approximately 20 ms
84**	Sweep-dwell time approximately 200 ms
85**	Sweep-dwell time approximately 1 s
86**	Display sweep-start frequency
87**	Display sweep-stop frequency

Note 1: When the options code is displayed the fitting of an option is indicated by the allocated frequency display digit being set to '1'. The digit allocation is:

1	2	3	4	5	6	7	8	9	10
Always	GPIB	33 address store	100 address store	Always 0	Auxiliary Control Unit	Always 0	RPPU	Always 0	Always ....

Note 2: When the special functions codes is displayed, the enablement of a function is indicated by the allocated frequency-display digit being set as shown.

1	2	3	4	5	6	7	8	9	10
Always	1=42	1=43	0=73 1=74	Always 0	0=07 1=08	0=05 1=06	0=02 1=03	1=01	Always ....

Note 3: Special functions marked * are selected automatically on switching-on.

Special functions marked ** are cancelled by the operation of any primary function key or the entry of fresh data.

Special function 20 is cancelled by operating the spinwheel.

To cancel those special functions marked ** via the GPIB, send any primary function code with no data. Care must be taken over selecting the code to be used as additional, unwanted changes to the instrument's settings may occur.

Error Codes

4.5.22

Description This instruction describes how to read and interpret the error codes.

Procedure Generation of error is signalled by ERROR indicator flashing

Press [DISPLAY ERROR CODE] and hold to read error code

Read error code from memory display.

Those codes marked * cannot be cleared until the cause of error has been removed. Other codes are cancelled automatically after they have been read or if a new data entry is made.

Keys and Program Codes

GPIB

Keys	Codes
DISPLAY ERROR CODE	WY

Indications The ERROR indicator flashes when an error code is generated.

The error code number appears in the memory display and the ERROR indicator is lit when the DISPLAY ERROR CODE key is held pressed.

The ERROR indicator is reset and the memory display returns to normal when the key is released, except in the case of those errors which can only be cleared by removal of the cause of error.

Comments

The interpretation of the error codes is as follows:

Code	Error
00	No error
01*	Microprocessor RAM error on initialization
02*	ROM error: frequency display shows faulty ROM number
03*	Stuck key on initialization: frequency display shows code of stuck key
09*	RPPU tripped. Reset by switching carrier on
10	Frequency entry excessive: output set to 1.3 GHz
11	Frequency entry too low: output set to 10 kHz
12	Relative frequency offset too high: offset set to give output of 1.3 GHz
13	Relative frequency offset too negative: offset set to give output of 10 kHz
14	Frequency step-size entry excessive: reset to 1299.990 MHz
15	Amplitude entry excessive: output set to 2.00 V (+19 dBm)
16	Amplitude entry too low: output set to 22.4 nV (-140 dBm)
17	Relative amplitude offset too high: offset set to give output of 2.00 V (+19 dBm)
18	Relative amplitude offset too negative: offset set to give output of 22.4 nV (-140 dBm)
19	Amplitude step-size entry excessive: reset to 1.99 V or 159 dB
20*	FM deviation excessive for output frequency
21	FM-deviation entry excessive for frequency range: reset to maximum permissible value
22	Phase-deviation entry excessive: reset to 5.00 radians
23*	Phase modulation excessive for output frequency
24	AM-depth entry excessive: reset to 99%
25*	AM excessive for output amplitude
30*	FM/ØM-modulating signal level too low
31*	FM/ØM-modulating signal level too high
32*	AM/Pulse-modulating signal level too low
33*	AM/Pulse-modulating signal level too high
40	Key operation sequence error
41	Invalid use of spinwheel or step keys
42	Data input attempted when in Pulse mode
43	External DC input not permitted in phase mode
44	Exponential entry attempted for store, recall, or special functions
45	No step size set for frequency sweep
47	Invalid special-function code entered
50	Memory board not fitted
51	Error detected during memory test: frequency display shows faulty RAM number

Code	Error
52	Recalled memory location contains checksum error
53	Recalled memory location out-of-range
54	Incomplete memory address entered
55	MEM EXCH key operated in Store mode or Immediate Execute Recall mode
56	Write Protect set
57	Corruption of memory contents detected during test: frequency display shows corrupted location number
70	GPIB-letter command unknown
71	GPIB-numeric command out-of-range
72	GPIB learn-mode input interrupted and aborted
73	GPIB command interpreted while in standby mode
80*	Reference-generator loop out-of-lock
81*	Output loop out-of-lock
82*	Comb loop out-of-lock
83*	FM system PLL out-of-lock
84*	FM system FLL out-of-lock
88*	Output system AGC loop error or RF output unterminated
90*	Power supply - 15 V supply failure
91*	Power supply -5.2 V supply failure
92*	Power supply +5 V (D) supply failure
93*	Power supply +5 V (A) supply failure
94*	Power supply +15 V supply failure
95*	Power supply +24 V supply failure
96*	Power supply +18 V supply failure
97*	Power supply +24 V OVEN supply failure
99*	Overtemperature error - instrument switched to standby. To reset press STANDBY key.

Error code 73 will be cleared when the instrument leaves the standby mode. The instrument will be set according to the commands received while in standby.

Those codes marked * cannot be cleared until the cause of error has been removed. Other codes are cancelled automatically after they have been read or if a new data entry is made.

At some frequencies, if the RF output is not terminated, and a high output level is demanded, error 88 may be indicated. Normal operation is restored by terminating the output with 50 Ω.

GPIB

The error codes can be read via the GPIB using the instrument's status-data string.

Reverse Power Protection Unit

4.5.23

Description

This instruction describes how to use the reverse power protection unit (RPPU) option.

Operating Characteristics

Action: When tripped, the 9087's RF OUTPUT socket is latched in the open-circuit state. An audible warning is given.

Procedure

Operate the 9087 normally.
If the RPPU trips, disconnect the source of reverse power.

Switch the RF output on to reset the protection unit.

Keys and Program Codes

Keys	Codes
RF OUTPUT	OP1

Associated Error Codes

Code	Reason
09	RPPU tripped

Indications

When the RPPU is tripped, an audible warning is given and the RF output ON/OFF key indicator is extinguished.

Comments

The audible warning, but not the switching, of the RPPU can be tested using the special functions.

Related Instructions

Special Functions

SECTION 5 OPERATION VIA THE GPIB

5.1 PREPARATION FOR USE WITH THE GPIB

5.1.1 INTRODUCTION

5.1.1.1 The instrument must be prepared for use in accordance with the instructions given in Section 3 before the additional instructions given in this section are carried out.

5.1.2 CONNECTION TO THE GPIB

5.1.2.1 Connection to the GPIB is made via a standard IEEE 488 bus connector, mounted on the rear panel. The pin assignment is given in Table 5.1. An adaptor, Racal-Dana part number 23-3254, to convert the connector to the IEC 625-1 standard is available as an optional accessory.

TABLE 5.1

GPIB Connector Pin Assignment

Pin	Signal Line	Pin	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd. (6)
7	NRFD	19	Gnd. (7)
8	NDAC	20	Gnd. (8)
9	IFC	21	Gnd. (9)
10	SRQ	22	Gnd.(10)
11	ATN	23	Gnd.(11)
12	SHIELD	24	Gnd. (5 and 17)

5.1.3 ADDRESS SETTING

5.1.3.1 The interface address is set on five of six rear-panel-mounted switches. The sixth switch must be set to the logic '0' position (to the left as viewed from the rear of the instrument). The top switch is used to set the least significant address bit. The permitted address settings, in decimal and ASCII character form, are given in Table 5.2.

TABLE 5.2

Address Switch Settings

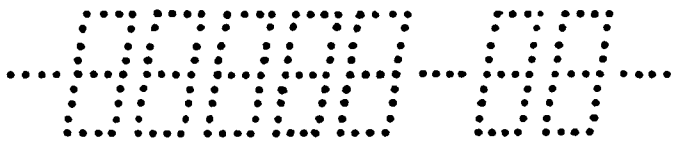
SWITCH SETTINGS					ADDRESS CODES			
A5	A4	A3	A2	A1	DECIMAL	ASCII LISTEN ADDRESS	ASCII TALK ADDRESS	
0	0	0	0	0	0	SP	@	
0	0	0	0	1	1	!	A	
0	0	0	1	0	2	"	B	
0	0	0	1	1	3	#	C	
0	0	1	0	0	4	$	D	
0	0	1	0	1	5	%	E	
0	0	1	1	0	6	&	F	
0	0	1	1	1	7	'	G	
0	1	0	0	0	8	(	H	
0	1	0	0	1	9	)	I	
0	1	0	1	0	10	*	J	
0	1	0	1	1	11	+	K	
0	1	1	0	0	12	,	L	
0	1	1	0	1	13	-	M	
0	1	1	1	0	14	.	N	
0	1	1	1	1	15	/	O	
1	0	0	0	0	16	Ø	P	
1	0	0	0	1	17	1	Q	
1	0	0	1	0	18	2	R	
1	0	0	1	1	19	3	S	Instrument despatched with this setting
1	0	1	0	0	20	4	T	
1	0	1	0	1	21	5	U	
1	0	1	1	0	22	6	V	
1	0	1	1	1	23	7	W	
1	1	0	0	0	24	8	X	
1	1	0	0	1	25	9	Y	
1	1	0	1	0	26	:	Z	
1	1	0	1	1	27	;	[	
1	1	1	0	0	28	<	\	
1	1	1	0	1	29	=	]	
1	1	1	1	0	30	>	^	

5.1.3.2 The instrument is despatched with the address switches set to decimal 19 (ASCII 3 (listen) and ASCII S (talk)). The address-set, in both binary and decimal format, can be displayed by pressing

SPECIAL FUNCT 4 0

when in local control or by sending the command DG40 via the GPIB. If the 9087 is in local control and in special function 40, the address display will be updated as the switches are changed.

5.1.3.3 When the sixth, (bottom switch) is put to the logic '1' position, the interface is switched to the listen-only mode. The settings of the upper five switches are then irrelevant. In this mode the instrument will accept all commands sent via the bus, and cannot be addressed to talk. If an attempt is made to display the address when in the listen-only mode, the frequency display will show:



5.2 DATA ACCEPTANCE MODES

5.2.1 When the 9087 is under remote control, two modes of accepting device-dependent commands generated at the controller are available. These are:

(a) The immediate mode

(b) The deferred mode

The mode to be used is selected by the operator, the deferred mode being selected automatically on switching-on.

5.2.2 When the instrument is operating in the immediate mode, each byte of an addressed command is processed as it is received, the following byte being accepted only when processing is complete. The bus is thus occupied for the data transfer and the data processing time. This method gives the fastest change in 9087 control setting when a slow controller is used. No end of string indication is required.

5.2.3 When operating in the deferred mode, strings of addressed commands are accepted and stored without change to the 9087's control settings. The bus is released and processing of the data is commenced when the end of string indication is received. The bus is therefore occupied for the time taken to transfer the data only, and better bus utilization is possible. The end of string indication may be CR, LF, ASCII X, ASCII x or the EOI line set low for the duration of the last byte. If a combination of these indicators is received all but the first will be ignored.

5.2.4 The input buffer used has a capacity of 256 bytes. If the command string is longer than this, data transfer will be stopped when the store is full. The bus will be held while the first 256 bytes are processed, after which data transfer will continue.

5.3 DISPLAY UPDATING

5.3.1 When the immediate mode of data acceptance is in use, each byte received is acted upon before the next byte is accepted. Since the time taken to update the display forms a significant part of the time required to process a byte, the system operating speed can be improved by reducing the frequency at which display updating occurs. The following three modes are available:

(a) Displays updated at the end of each data string recognized as a command. This mode is automatically selected on switching-on, or by using special function 41.

(b) Displays blanked. This permits the maximum operating speed. The complete display is blanked except for the amplitude display, which shows 42, and the GPIB indicators. The mode is selected using special function 42.

(c) Displays updated following the acceptance of each data byte. This corresponds to the form of updating used when the instrument is operating under local control. Although the operating speed is low, this mode can prove useful when checking the operation of the 9087 and the bus. The mode is selected using special function 43.

5.4 DATA OUTPUT

5.4.1 The instrument generates three different forms of data string related to its operating status and control settings. These are:

(a) The instrument-status data string

(b) The fast-learn-mode data string

(c) The long-learn-mode data string

5.4.2 The required form of output is obtained by setting the interface output mode by means of the appropriate code, sent as an addressed command, and then addressing the instrument to talk. The output mode will remain set until an alternative mode is set or the instrument is switched off. The mode giving the instrument-status data string is selected on switching-on.

5.5 THE INSTRUMENT STATUS DATA STRING

5.5.1 The data output mode giving the instrument-status data string is set using the addressed command IS. The string contains 27 bytes, consisting of:

(a) Six two-digit, decimal, error code numbers, each followed by a comma

(b) A three-digit, octal number, representing the setting of the status-byte mask register, followed by a comma.

(c) A three-digit, octal, special function number.

(d) CR and LF

The EOI line is set low for the duration of the transmission of LF. The first error code number in the string is the one appearing in the display.

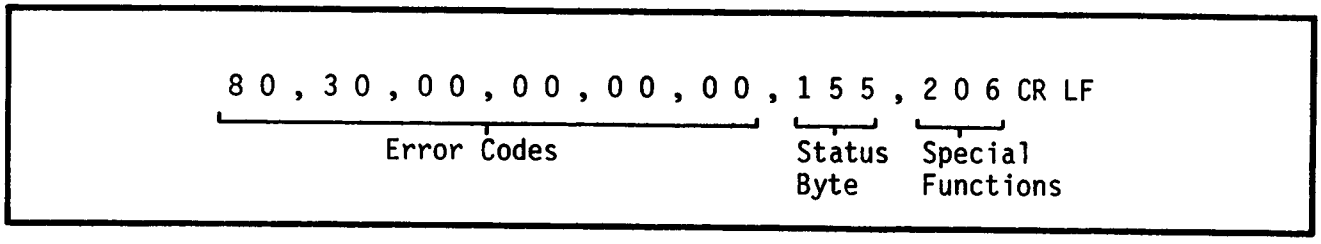


Fig. 5.1 Typical Status Data String

5.5.2 The error code numbers should be interpreted according to Table 4.9 in Section 4. The interpretation of the status-byte mask setting is given in paragraph 5.8. The special function number should be interpreted in accordance with Table 5.3, Table 5.4 and Table 4.8 of Section 4.

TABLE 5.3

Special Function Number Bit Allocation

First Digit	Second Digit	Third Digit
DN DE	STLK 0 IOL	DB BC FB

TABLE 5.4

Special Function Number Bit Code

Bit Settings	Function		Number of Special Function Enabled
DN DE			
0 0 0 1 1 0	Display options with remote control via GPIB		41 43 42
STLK			
0 1	Write Protect	OFF ON	73 74
IOL			
0 1	Out of lock error display	ON OFF	07 08
DB			
0 1	Auxiliary input debounce	ON OFF	05 06
BC FB			
X 1 0 0 1 0	Front panel annunciator selection	OFF CLUNK BEEP	01 02 03

5.6 THE LEARN MODE

5.6.1 INTRODUCTION

5.6.1.1 The learn mode provides a means of resetting the controls of the 9087 rapidly, using predetermined data strings. The data strings are produced in the 9087, the content of a string being governed by the control settings in use at the time the string is generated. The strings are fed via the bus to an external store, which must be provided as part of the bus system. The store must be capable of handling 8-bit binary data. When a data string is fed back to the 9087 as an addressed command, the control settings will be returned to those in use when the data string was generated.

5.6.1.2 Two lengths of data string are possible. The shorter string, of 13 bytes, controls the frequency setting only. The longer string, of 61 bytes, controls the complete range of instrument settings. Each string includes a header, which indicates the length of the string, @9 being used for the shorter string and @A for the longer. The form of string generated can be selected by the operator using the appropriate interface output-mode code.

5.6.1.3 When a data string is transmitted from the 9087 to store, the EOI line is set low for the duration of the final byte. No CR or LF is transmitted. If no action is taken to stop the acceptance of data, the data string will be repeated continuously.

5.6.1.4 When a learn-mode data string is transmitted back to the 9087, the header is recognised, and the instrument enters the learn mode automatically. For the fast learn mode the frequency display shows ten decimal points. The header indicates the number of bytes in the string. No end of string indicator should be added. It is essential that no interruption of the string occurs during transfer.

5.6.1.5 Once a learn-mode data string has been received, the 9087 will remain in the learn mode until an addressed command not commencing with the ASCII character @ is received. It will then revert to the immediate or deferred mode, according to which was last selected.

5.6.2. OBTAINING A DATA STRING OUTPUT

5.6.2.1 When operating in the remote control mode, a data string output is obtained as follows:

(a) Address the 9087 to listen.

(b) Send the addressed command LM1 or LM2, according to the length of data string required.

(c) Address the store which is to accept the data string to listen.

(d) Address the 9087 to talk.

(e) Stop the data transfer when the string has been stored by sending the UNTALK command.

5.6.2.2 The 9087 will only transmit a learn-mode data string under the control of the bus controller. However, it is frequently more convenient to set up the content of the data string using the front panel in the local control mode. The following procedure will permit the process to be controlled from the 9087:

(a) Set the 9087's status-byte mask, as instructed in paragraph 5.8.3, such that bit 7 (SRQ) and bit 8 (operator requests response) of the status byte are enabled.

(b) Program the controller such that, after detecting SRQ, conducting a serial poll, and receiving a status byte with bits 7 and 8 at '1' from the 9087 it will:

(i) address the 9087 to listen

(ii) send the addressed command LM1 or LM2, according to which length of data string is required. Address the store which is to receive the data string to listen

(iii) address the 9087 to talk

(iv) send ATN false

(v) stop the data transfer when the string has been stored by sending the UNTALK command.

(vi) return the 9087 to local control, ready for a further data string to be set up, if required.

(c) Set up the 9087 controls to the required pattern.

(d) Press [SPECIAL FUNCT] [4] [4].

This will cause the 9087 to send the SRQ message, resulting in a serial poll followed by the transfer of a data string to store.

5.7 MONITORING THE CONTROL SETTINGS

5.7.1 It is possible to read, and if necessary record, the 9087's function and output settings by making use of the learn-mode data strings. In practice, because of the complex nature of the short data string, it will be found to be more convenient to use the long string even when information relating to frequency setting only is required.

The data string is obtained from the 9087 as previously described. The bytes should be interpreted as shown in Table 5.5

TABLE 5.5

Long-Learn-Mode Data String Interpretation

Byte Number		Data Format
1 and 2	Header	Byte 1 = @ Byte 2 = A
3	Modulation control	See Table 5.7
4	AM control	See Table 5.8
5	FM control	See Table 5.9
6	ØM control	See Table 5.10
7	Pulse modulation control	See Table 5.11
8	AM depth	2 digits
9 to 11	FM deviation	6 digits
12 and 13	ØM deviation	3 digits
14	Incremental controls	See Table 5.12
15	REL and sign data	See Table 5.13
16 to 20	Reference frequency	10 digits
21 to 25	Relative frequency	10 digits
26 to 30	Output frequency	10 digits
31 to 35	Frequency step size	10 digits
36 and 37	Amplitude step size	4 digits
38 and 39	Reference amplitude (dB)	4 digits
40 and 41	Relative amplitude (dB)	4 digits
42 and 43	Output amplitude (dB)	4 digits
44 to 49	Reference amplitude (V)	12 digits
50 to 55	Relative amplitude (V)	12 digits
56 to 61	Output amplitude (V)	12 digits

Note: (1) Numerical data are in packed BCD, two digits per byte. The format is as shown in Table 5.6.

(2) Full numerical data are given for FM deviation, reference amplitude (volts), and output amplitude (volts). The data are rounded to three significant figures to provide the control signals for the 9087's output and displays.

(3) In Tables 5.7 to 5.13 a bit set to logic '1' indicates a selected condition.

TABLE 5.6

Numerical Data Format

Byte	DIO8 7 6 5 MSB LSB	4 3 2 1 MSB LSB
First ↓ Last	Most significant digit ↓ Penultimate digit	Second digit ↓ Least significant digit

TABLE 5.7

Modulation Data

Bit Number							
8	7	6	5	4	3	2	1
-	-	CAL? indicator	-	ØM	Pulse modulation	FM	AM

TABLE 5.8

AM Control Data

Bit Number							
8	7	6	5	4	3	2	1
-	-	Pulse mod set	AM ON	AM INT 400Hz	AM INT 1kHz	AM EXT AC	AM EXT AC

TABLE 5.9

FM Control Data

Bit Number							
8	7	6	5	4	3	2	1
-	-	ØM set	FM ON	FM INT 400Hz	FM INT 1kHz	FM EXT AC	FM EXT DC

TABLE 5.10

ØM Control Data

Bit Number							
8	7	6	5	4	3	2	1
-	-	-	ØM ON	ØM INT 400Hz	ØM INT 1kHz	ØM EXT AC	-

TABLE 5.11

Pulse Modulation Control Data

Bit Number							
8	7	6	5	4	3	2	1
-	-	-	Pulse ON	Pulse INT 400Hz	Pulse INT 1kHz	Pulse EXT AC	Pulse EXT DC

TABLE 5.12

Incremental Control Data

Bit Number							
8	7	6	5	4	3	2	1
-	-	Output ON	Coarse	Medium	Fine	Hold	Step

TABLE 5.13

REL and Sign Data

Bit Number							
8	7	6	5	4	3	2	1
Freq. system in rel. mode	Amp. system in rel. mode	Freq. rel. sign 0=+ve 1=-ve	Amp. rel. sign 0=+ve 1=-ve	Amp. ref. sign 0=+ve 1=-ve	Amp. output sign 0=+ve 1=-ve	Amp. display mode 0=dB 1=V	Amp. step mode 0=dB 1=V

5.8 SRQ AND STATUS BYTE OUTPUTS

5.8.1 STATUS BYTE FORMAT

5.8.1.1 The status byte is transmitted via the GPIB by the 9087 in response to a serial poll. The byte should be interpreted as shown in Table 5.14.

TABLE 5.14

Status Byte

Bit Number							
8	7	6	5	4	3	2	1
Operator requests response	RQS	Syntax error	End of sweep	Entry error	Hardware failure	0	External inputs out-of-range

5.8.2 STATUS BYTE MASK REGISTER

5.8.2.1 The circumstances under which the 9087 will send the SRQ message and the content of the status byte are both governed by the contents of the status-byte mask register. The mask register contains eight bits, corresponding to the eight bits of the status byte. If a mask register bit is at logic '1' the corresponding bit of the status byte is enabled and will reflect the instrument's status. When a mask register bit is at logic '0' the generation of the corresponding bit of the status byte is inhibited.

5.8.2.2 In the case of bit 7, a logic '1' in the mask register will result in the RQS indication being included in the status byte. The SRQ message will then be sent true if any bit in the status byte is set. A logic '0' in this position in the mask register will prevent the RQS indication appearing, and will also disable the generation of the SRQ message.

5.8.3 SETTING THE MASK REGISTER

5.8.3.1 Entries are made into the mask register by means of an addressed command consisting of the alpha characters RS followed by three octal digits. The first digit is limited to 0 to 3, and relates to bits 8 and 7. The second and third digits may be from 0 to 7, the second digit relating to bits 6, 5 and 4 and the third digit to bits 3, 2 and 1. An entry of RS 277, for example, will inhibit the RQS indication and the generation of the SRQ message, but will enable all the other status byte bits. On switching-on the mask is set to 155.

5.8.1 READING THE MASK REGISTER

5.8.1.1 The setting of the mask register is included in the instrument-status data string, and may be read via the GPIB as instructed in paragraph 5.5.

5.9 REMOTE/LOCAL CHANGEOVER

5.9.1 LOCAL TO REMOTE CONTROL CHANGEOVER

5.9.1.1 The 9087 is switched from local to remote control by the following sequence of control and data line messages:

(a) Remote enable (REN) true (low).

This primes the remote control enable, but the 9087 remains in local control. REN must remain true if any instrument on the bus is to remain in remote control.

(b) Attention (ATN) true (low).

(c) Listen address.

The 9087 enters the listener-addressed state (LADS) on recognition of its listen address.

(d) ATN false (high).

The 9087 enters the listener-active state (LACS) after a delay, and enters the remote state (REMS) on receipt of the first data byte.

5.9.1.2 No change to any of the 9087 control settings occurs on changeover from local to remote control.

5.9.2 REMOTE TO LOCAL CONTROL CHANGEOVER

5.9.2.1 The 9087 will be switched from remote to local control on:

(a) Operation of the front-panel LOCAL key. This is effective only if local lockout is not set.

(b) Receiving the go-to-local (GTL) command when in the LADS.

(c) Receiving the REN message false (high). This is independent of the addressed state of the 9087.

5.9.2.2 No change to any of the 9087's control settings occurs on changeover from remote to local control.

5.9.3 LOCAL LOCKOUT (LLO)

5.9.3.1 Operation of the front-panel LOCAL key during the transfer of data to the 9087 could result in the instrument being switched from remote to local control with the control settings in an unknown state. To prevent this the LOCAL key can be disabled by setting local lockout.

5.9.3.2 Local lockout may be set at any time when the REN message is true (low). The recognition of the LLO message is not dependent on the addressed state of the instrument. Apart from the disablement of the LOCAL key it causes no changes to the operation of the 9087. The only method of cancelling LLO is to send the REN message false (high). This affects all instruments or the bus, putting them to the local control state (LOCS).

5.10 LOGIC LEVELS

5.10.1 The control, handshake and data lines operate at standard +5 V TTL levels. Negative logic is used, i.e., logic '1' is represented by a level $\leq$0.8 V and logic '0' by a level of $\geq$2 V.

5.11 GPIB COMMAND EXECUTION TIME

5.11.1 The following paragraphs provide information regarding the time required for the 9087 to receive and respond to a command sent via the GPIB, and the time for which the bus is busy during the operation. The total delay in executing a command is determined by the time taken to accept the command, and the processing and settling times needed by the 9087 to reach the required output state. These factors depend upon:-

(a) the data-acceptance mode, and

(b) the display-updating-mode in use.

5.11.2 IMMEDIATE AND DEFERRED DATA ACCEPTANCE MODES

5.11.2.1 The acceptance times per character for the immediate and deferred modes are shown in Table 5.15.

TABLE 5.15

Character Acceptance Times

Character	Immediate Mode	Deferred Mode
Letters	0.50 ms	0.43 ms
Numbers	0.76 ms	0.43 ms
Symbols	0.65 ms	0.43 ms

5.11.2.2 The processing time depends upon the nature of the command, and not necessarily on the number of characters received. The processing times required for certain typical commands are given in Table 5.16, and these times, combined with the required data acceptance times, are given in Table 5.17.

TABLE 5.16

Processing Times

Command	Normal Display Update		No Display Update	
	Immediate	Deferred	Immediate	Deferred
MRØØME	30.2 ms	24.3 ms	20.7 ms	21.9 ms
FQ1.234567890GZ	7.1 ms	9.4 ms	2.0 ms	7.0 ms
AP-123DB	22.2 ms	21.9 ms	17.6 ms	19.6 ms
AM98%MA1MA4	11.1 ms	7.8 ms	3.0 ms	5.7 ms
FM68KZMF1MF4	11.2 ms	7.0 ms	2.0 ms	4.7 ms

TABLE 5.17

Processing Plus Data Acceptance Times

Command	Normal Display Update		No Display Update	
	Immediate	Deferred	Immediate	Deferred
MRØØME	33.8 ms	26.9 ms	24.2 ms	24.5 ms
FQ1.234567890GZ	17.4 ms	15.9 ms	12.3 ms	13.5 ms
AP-123DB	27.1 ms	25.3 ms	22.5 ms	23.0 ms
AM98%MA1MA4	17.8 ms	12.5 ms	9.7 ms	10.4 ms
FM68KZMF1MF4	18.2 ms	12.2 ms	9.0 ms	9.9 ms

5.11.2.3 The processing time includes the time devoted to updating the display. This occurs once-only per command string in the deferred mode, following the recognition of a valid command-string terminator, but may occur more than once in each command string when operating in the immediate mode. For this reason, when normal display updating is used, the processing time is less in the deferred mode. The saving in time will be greater than that indicated in Table 5.17 when command strings containing more than one command are used.

5.11.2.4 If display updating is inhibited by the enablement of special function 42, the processing time for the immediate mode is less than that for the deferred mode. This is because there is no saving in the time taken to update the display, but time is used in the deferred mode to store the characters as they are received, and to recall them for processing once the command string terminator is recognized.

5.11.2.5 Settling time must be allowed in addition to the data acceptance and processing times. The time required for this depends upon the nature and magnitude of the change made.

5.11.2.6 The times for which the bus is busy during the receipt and execution of typical commands are shown in Table 5.18. It can be seen that the use of the deferred mode permits better bus utilization.

TABLE 5.18

Bus Busy Times

Command	Normal Display Update		No Display Update	
	Immediate	Deferred	Immediate	Deferred
MRØØME	11.2 ms	2.6 ms	3.8 ms	2.6 ms
FQ1.234567890GZ	12.8 ms	6.4 ms	10.5 ms	6.4 ms
AP-123DB	7.5 ms	3.4 ms	5.2 ms	3.4 ms
AM98%MA1MA4	14.6 ms	4.7 ms	8.5 ms	4.7 ms
FM68KZMF1MF4	15.6 ms	5.2 ms	8.8 ms	5.2 ms

5.11.3 THE FAST LEARN MODE

5.11.3.1 In the fast learn mode, the data input to the 9087 always consists of a string of 13 bytes. The total execution time required is the sum of

(a) 460 µs data-acceptance-time

(b) 90 µs for data transfer within the 9087

(c) 400 µs settling time.

5.11.3.2 Since the processing time is 770 µs, the receipt of a second string may commence before settling is complete. Operation at the maximum rate is illustrated in Fig. 5.2.

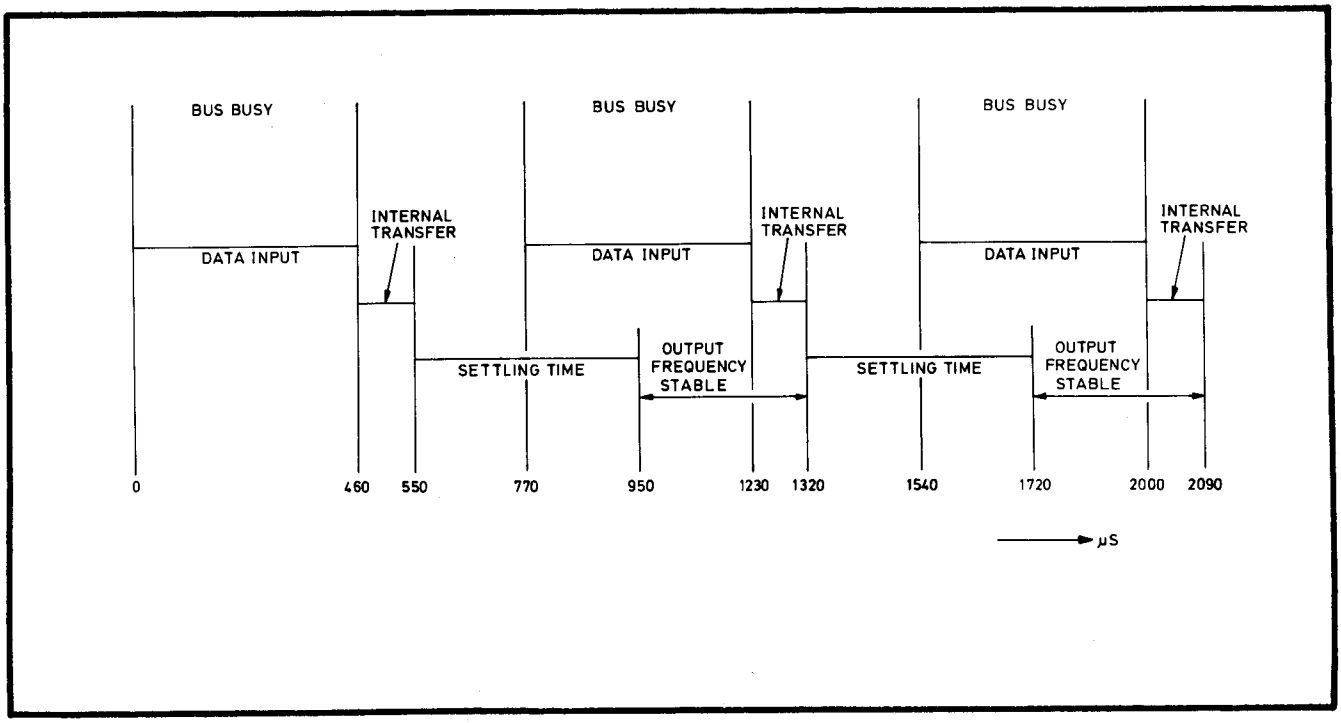


Fig. 5.2 Fast-Learn Mode Timing

5.11.4 THE LONG LEARN MODE

5.11.4.1 In the long learn mode, the data input to the 9087 always consists of a string of 61 bytes. The total execution time required is the sum of

(a) 1.97 ms data-acceptance-time

(b) 7.83 ms for data processing within the 9087

(c) Settling time dependent upon the nature and magnitude of the output changes made.

5.11.4.2 The total processing time, which must be allowed to elapse before the receipt of a second data string commences, is 12.23 ms with normal display updating or 10.00 ms if display updating is inhibited.

5.12 OPERATING INSTRUCTIONS FOR REMOTE CONTROL

5.12.1 OPERATING MODES

5.12.1.1 The 9087 can be operated via the GPIB in either the addressed mode or the listen-only mode. In the addressed mode, the instrument's functions and RF output can be controlled by means of device-dependent commands, sent via the bus, when the instrument is addressed to listen; and data regarding the instrument's status or output can be read when the instrument is addressed to talk. In the listen-only mode, the instrument will accept all commands sent via the bus, and cannot be addressed to talk.

5.12.2 COMMAND CODES FOR REMOTE CONTROL

5.12.2.1 When the 9087 is addressed to listen, or is in the listen-only mode, it can be controlled by means of the device-dependent commands listed in Tables 5.19 to 5.27. In commands containing numerical data, the use of the decimal point is optional. If required, spaces, commas, and semicolons may be included in commands or command strings as an aid to clarity without affecting the operation of the 9087.

5.12.2.2 It is essential that the operation of the instrument using the front-panel controls, as described in Section 4, is understood before operation using the GPIB is attempted.

TABLE 5.19

Frequency Commands

Function	Function Code	Data	Units or Exponent
Set frequency	FQ	Up to 10 digits and DP	GZ, MZ, KZ, HZ or E± 2 digits
Set frequency step	FS		
Set relative frequency offset	FR		
Frequency step-up	FU		
Frequency step-down	FD		

Note: For the exponent format the unit of entry is Hz.

TABLE 5.20

Amplitude Commands

Function	Function Code	Data	Units or Exponent
Set amplitude	AP	Up to 4 digits and DP	VO, MV, UV, NV, ±dB or E± 2 digits
Set amplitude step	AS		
Set relative amplitude offset	AR		
Amplitude step-up	AU		
Amplitude step-down	AD		

Note: For the exponent format the unit of entry is volts.

TABLE 5.21

Modulation Commands

Function	Function Code	Data	Units or Exponent
Set AM depth	AM	Up to 2 digits	%, PC, E± 2 digits
Set FM deviation	FM	Up to 3 digits and DP	MZ, KZ, HZ or E± 2 digits
Set ØM deviation	HM	Up to 3 digits and DP	RD or E± 2 digits
Select pulse modulation	PM		
AM control	MA	1 digit from Ø to 5	
FM control	MF	1 digit from Ø to 5	
ØM control	MH	1 digit from Ø to 4	
Pulse modulation control	MP	1 digit from Ø to 5	

Note: (1) For the exponent format the units of entry are:
(a) % for AM
(b) Hz for FM
(c) radians for ØM

(2) The coding for the control data is:
Ø = Modulation off
1 = Modulation on
2 = Select internal 400 Hz source
3 = Select internal 1 kHz source
4 = Select external source, AC coupled
5 = Select external source, DC coupled

TABLE 5.22

Memory Commands

Function	Function Code	Memory Address	Execute
Store front-panel settings	MS	2 digits	ME
Recall front-panel settings	MR	2 digits	
Set instrument to recalled settings			ME
Memory exchange	MR	2 digits MI 2 digits	ME
Recall, display, and set a stored pattern	MR ME	2 digits	

Note: The memory exchange sequence does not affect the RF output of the 9087. The display will show the first memory location contents when the first address is entered and the second location contents when the second address is entered. The exchange is implemented by the 9087 ME command, and the display then reverts to the current instrument settings.

TABLE 5.23

Data Acceptance Mode Codes

Mode	Code
Deferred	RM1
Immediate	RM2

Note: When the deferred mode is in use, an end-of-string indication is required. This may be CR, LF, ASCII X, ASCII x or the EOI line set low (true) for the duration of the final byte.

TABLE 5.24

Data Output Mode Codes

Function	Code
Send instrument-status data string when addressed to talk	IS
Send long-learn-mode string when addressed to talk	LM1
Send fast-learn-mode string when addressed to talk	LM2

Note: The sending of the status byte in response to a serial poll is not affected by the output mode code.

TABLE 5.25

Status-Byte Mask-Setting Code

Function	Function Code	Data
Set status-byte mask	RS	3 octal digits

TABLE 5.26

Increment System Commands

Function	Code
Spinwheel HOLD off	IN Ø
Spinwheel HOLD on	IN 1
COARSE sensitivity	IN 2
MEDIUM sensitivity	IN 3
FINE sensitivity	IN 4
STEP selected	IN 5

TABLE 5.27

Miscellaneous Codes

Function	Code
Switch to standby	GS 1
Cancel standby	GS Ø
Carrier on	OP 1
Carrier off	OP Ø
Initialize	IP
Enable special function	DG 2 digits of special function number
Display error code	WY

Note: (1) The device clear (DCL) or selected device clear (SDC) messages may be substituted for code IP

(2) The special functions are listed in Section 4, Table 4.8. To exit from those special functions marked** send any primary function code.

TABLE 5.28

Alphabetic List of Function Codes

Code	Meaning	Code	Meaning
AD	Amplitude step-down	IP	Initialize
AM	Amplitude modulation	IS	Status data string
AP	Amplitude	LM	Learn-mode data string
AR	Amplitude, relative	MA	AM control
AS	Amplitude step-size	ME	Memory execute
AU	Amplitude step-up	MF	FM control
DG	Special function	MH	Phase-modulation control
FD	Frequency step-down	MI	Memory Exchange
FM	Frequency modulation	MP	Pulse-modulation control
FQ	Frequency	MR	Memory recall
FR	Frequency, relative	MS	Memory store
FS	Frequency step-size	OP	Carrier control
FU	Frequency step-up	PM	Pulse modulation
GS	Standby	RM	Data acceptance mode
HM	Phase modulation	RS	Status-byte mask
IN	Increment	WY	Display-error code

TABLE 5.29

Alphabetic List of Units Codes

Code	Units	Code	Units
DB	dB	MZ	MHz
E	Exponent	NV	nV
GZ	GHz	PC	%
HZ	Hz	RD	Radians
KZ	kHz	UV	µV
MV	mV	VO	V
		%	%

SECTION 6 PRINCIPLES OF OPERATION

6.1 INTRODUCTION

6.1.1 This section is written in two parts. Paragraph 6.4 covers the operating principles of the 9087 in general terms, with reference to the block diagram, Fig. 6.1. Paragraph 6.5 describes the operation of the circuits in greater detail, with reference to the circuit diagrams given in Section 8.

6.1.2 In the circuit descriptions the integrated circuits are referred to by the circuit reference given on the appropriate circuit diagram. Note that a separate series of numbers, starting at IC1, is allocated to each assembly. Where an integrated circuit package contains more than one circuit, suffix letters are used to distinguish between them. Where it is required to identify a particular pin of an integrated circuit, the circuit reference, with suffix letter if appropriate, is followed by an oblique stroke and the required pin number.

6.2 PHYSICAL CONSTRUCTION

6.2.1 A number of the power supply components are mounted directly onto the chassis. The remainder of the circuits are carried on printed circuit boards (PCBs), each of which is allocated an assembly number. Some of the PCBs are mounted on the chassis, as shown in Section 8, Fig. 1. The remainder are contained within the attenuator, the internal frequency standard, or the sealed units of the module pack, which is illustrated in Section 8, Fig. 2.

6.3 SERVICING THE SEALED MODULES

6.3.1 This manual contains no technical description or servicing information regarding the attenuator, the internal frequency standard, or the sealed units of the module pack. In the event of failure of any of these assemblies it should be returned to Racal-Dana Instruments, or their agents, for repair and calibration. The breaking of the seal on any of these units will invalidate any warranty given by Racal-Dana Instruments.

6.4 PRINCIPLES OF OPERATION

6.4.1 FUNCTIONAL SYSTEMS

6.4.1.1 It will be seen from the block diagram, Fig. 6.1, that the circuits of the 9087 can be grouped into three functional systems as follows:

(a) The generating system for the RF output
(b) The control, memory, and display system
(c) The power supply system.

6.4.2 THE RF GENERATING SYSTEM

6.4.2.1 The RF generating system synthesizes the required output carrier frequency from a single standard-frequency input. This input may be derived from the internally mounted frequency standard, or may be connected at a rear panel mounted socket. The standard frequency input is fed to the reference generator and LF synthesizer module, 19-1047.

6.4.2.2 The reference generator section of the module produces signals of 100 MHz, 10 MHz, 1 kHz and 400 Hz, all locked to the frequency standard. The 100 MHz and 10 MHz outputs form the reference signals for phase-locked loops in the FM system and comb loop modules. The 1 kHz and 400 Hz outputs are the internal modulation signals, and are fed to the audio system assembly.

6.4.2.3 The LF synthesizer section of the module contains a series of phase-locked loops, and provides an output which can be varied from 10 MHz to 15 MHz in 1 Hz steps. The actual frequency generated is set by the LF synthesizer control signals from the control system.

6.4.2.4 When FM or ØM is in use the appropriate deviation is added to the LF synthesizer output in the FM system module, 19-1046. The modulating signal is provided by the audio system assembly, 19-1048. The form and amplitude of the deviation is controlled by signals fed to this unit from the control system via the data and address buses. The modulating signal may be derived from either of the audio outputs from the reference generator or from an external source.

6.4.2.5 The output of the FM system module is fed to the comb loop module, 19-1045. Within the module a phase-locked loop, using the 100 MHz signal from the reference generator, synthesizes a signal which can be varied between 390 MHz and 1310 MHz in 10 MHz steps. The frequency is controlled by signals fed to the module from the control system. A second phase-locked loop adds the signal from the first loop to the input from the FM system module. This gives an output which can be varied from 400 MHz to 1.3 GHz in 1 Hz steps, and which is deviated according to any FM or phase modulation in use.

6.4.2.6 The output of the comb loop module passes to the output system module, 19-1044. Here the lower frequency ranges of RF output are generated, either by frequency division or by mixing the input to the module with frequencies derived from the 100 MHz output of the reference generator. The module also contains the modulators used for pulse and amplitude modulation. The modulating signal is obtained from the audio system assembly, and may be derived from either of the audio outputs of the reference source generator or from an external source.

6.4.2.7 The RF signal from the output system module is amplified in the RF output amplifier, which is contained within the attenuator module, 11-1526. The amplified signal passes to the RF output socket via the microprocessor-controlled, stepped attenuator and the reverse-power protection-unit option, if this is fitted.

6.4.2.8 The coarse setting of the output amplitude is made using the stepped attenuator. Intermediate values are obtained by means of a microprocessor-controlled amplitude modulator within the output system module. Once set the level is maintained by means of an automatic gain control system. The control voltage for this is derived from a peak detector at the output of the RF amplifier, and is fed back to the modulator in the output system module.

6.4.3 THE CONTROL, MEMORY AND DISPLAY SYSTEM

6.4.3.1 The control, memory, and display system comprises five assemblies, which are interconnected by the instrument address and data buses, and a keyboard, which is connected to the system by the keyboard address and data buses. The system provides the means of controlling the instrument, either by means of the keyboard or via the GPIB, and of reading the current instrument settings and status, either by means of a front-panel display or via the GPIB.

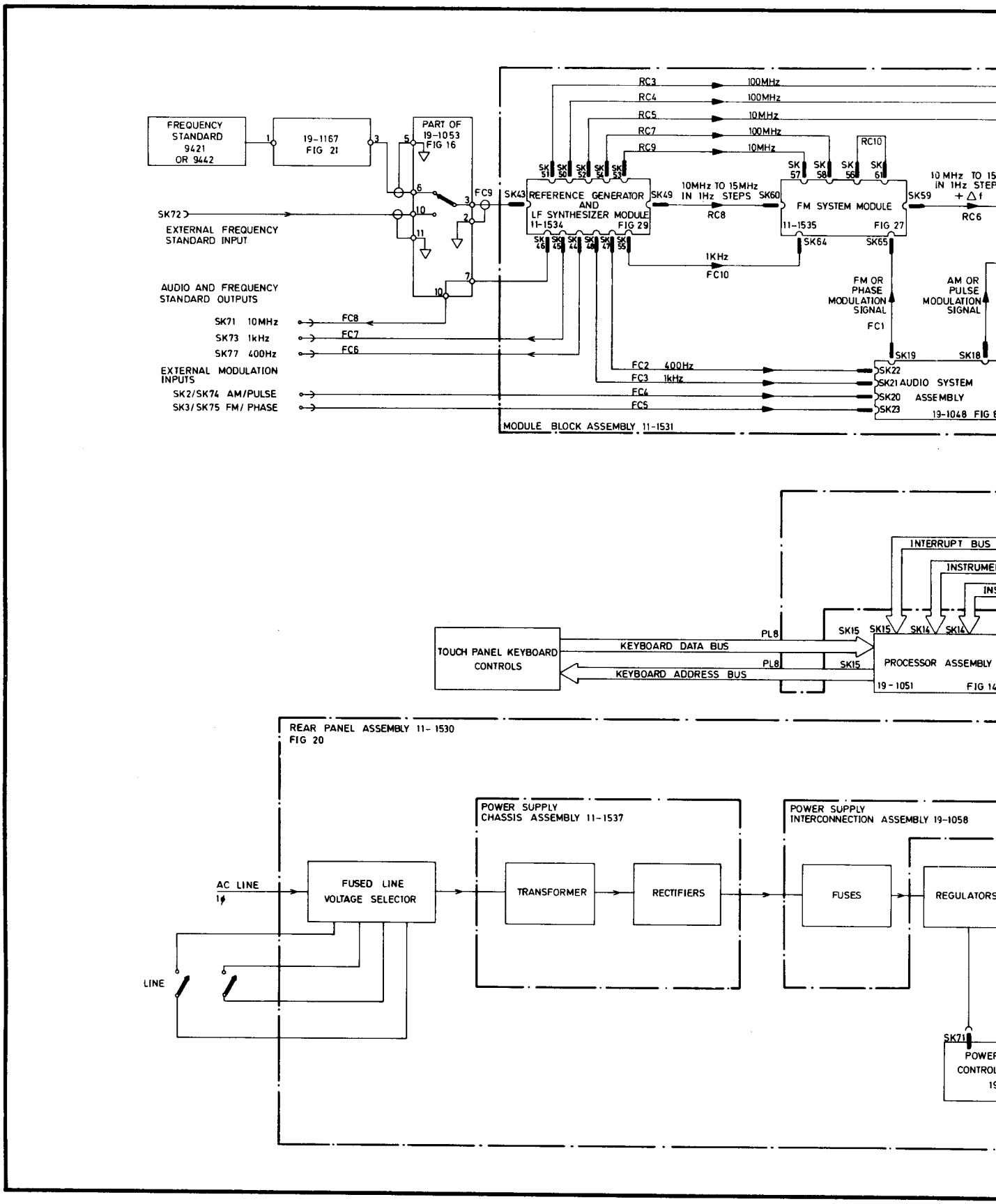
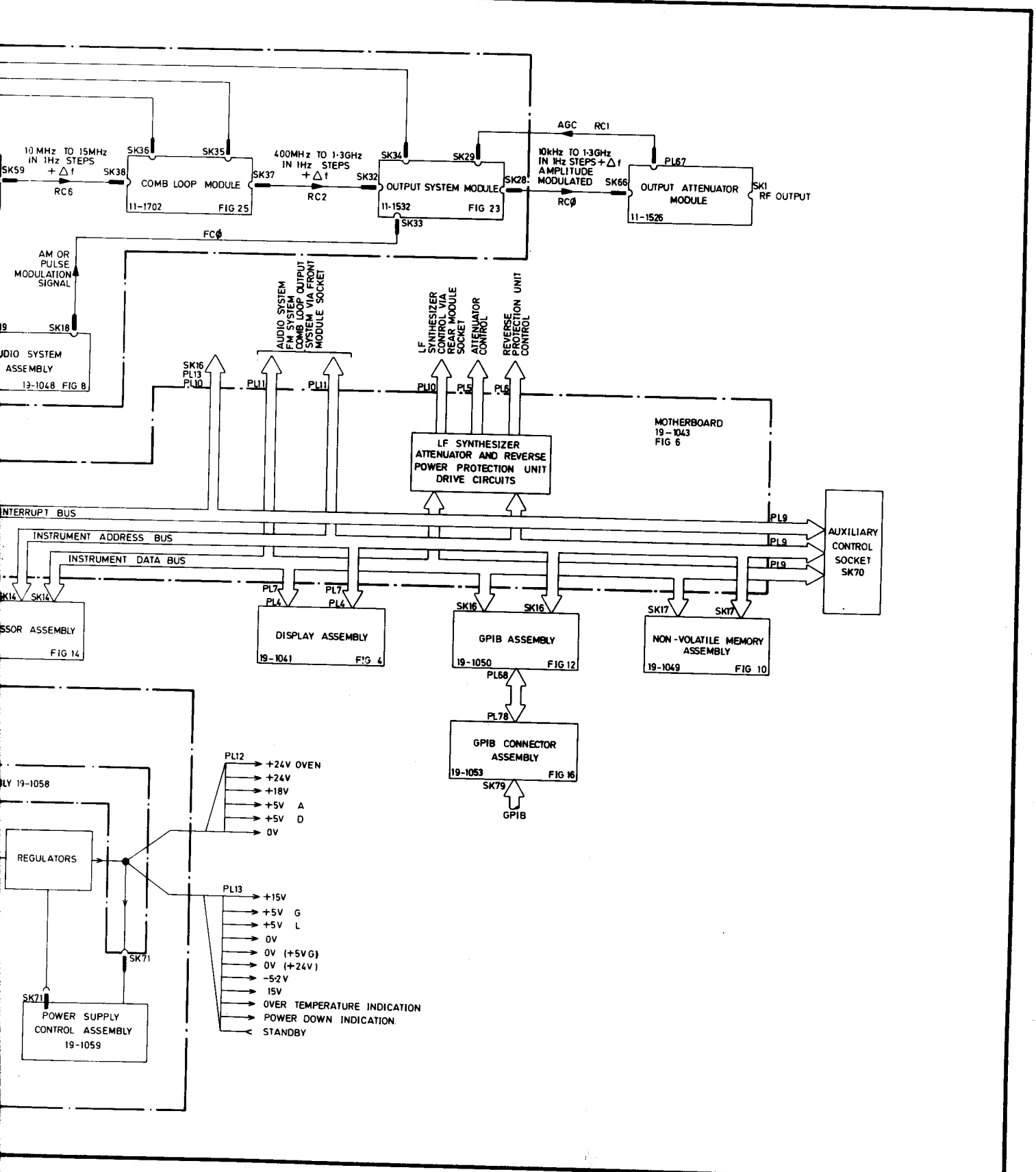


Figure 6.1 Bloc



1 Block Diagram

6.4.3.2 The operation of the assemblies within the 9087 is determined by the data held in latches within the assemblies. The data to be entered in the latches and the latch addresses are transmitted by the processor assembly, 19-1051, via the instrument's data and address buses. The address decoding for the LF synthesizer, the RF output attenuator, and the reverse-power protection unit takes place on the motherboard, 19-1043, but in all other cases decoding takes place in the assembly containing the addressed latch.

6.4.3.3 The processor assembly operates under the control of a 6802 microprocessor, in accordance with a program held in read-only memory (ROM) located on the processor assembly. The microprocessor is interrupt-controlled.

6.4.3.4 The keyboard is of the pressure-sensitive type, and features an 8 x 8 key matrix. Each key operation generates an interrupt request (IRQ) and is processed individually by the processor system, using the keyboard address and data buses.

6.4.3.5 The display assembly, 19-1041, features three different types of indicators. Numerical indicators are used to display frequency, output amplitude, modulation parameters, store locations, and error codes. Illuminated legends and LED indicators are used to show the units of the display, and the front-panel control settings currently in use. Each indicator is controlled by a separate data latch, but all the data latches are updated every time a change to the display is made.

6.4.3.6 A non-volatile random-access memory (RAM) is provided on assembly 19-1049. This memory can be used to store and recall complete instrument settings. When the instrument is switched off, or if power fails, the current instrument settings are written into this memory in location 00. The pattern stored in this way will be recalled when the instrument is switched on or when power is restored.

6.4.3.7 The GPIB assembly, 19-1050, and the GPIB connector assembly, 19-1053, provide an interface to the IEEE-488-GPIB. The interface is able to distinguish between universal and addressed commands, recognize the instrument's talk and listen addresses, and generate the signals required by the handshake protocol without involvement of the microprocessor. An interrupt will be generated for each of the following situations:

(a) A device-dependent data byte is held in the data-in register for the microprocessor to read.

(b) The last device-dependent data byte loaded into the data-out register has been read by the bus.

(c) DCL or SDC received.

(d) GET received.

(e) UNTALK or UNLISTEN received.

(f) IFC received.

(g) Instruction to change the remote/local status (RLC) received. This may be the GTL command when in the remote control mode or the unit's listen address when in the local control mode.

6.4.3.8 The program enabling the microprocessor to control the GPIB interface is carried in a ROM on the GPIB interface assembly.

6.4.4 THE POWER SUPPLY SYSTEM

6.4.4.1 The high-voltage AC circuits of the power supply are carried on the instrument's rear-panel assembly, 11-1530, while the remaining circuitry is carried on the power-unit chassis assembly, 11-1537. With the exception of the +24 V (OVEN) regulator, the regulators and rectifiers are mounted directly on the chassis. The other components are mounted on two PCBs, the interconnection assembly 19-1058 and the control assembly 19-1059.

6.4.4.2 In addition to the power supplies, the system provides warning outputs in the event of excessive temperature rise in the system or failure/switching off of the AC supply.

6.4.4.3 The application of a logic '1' level from the control system at the STANDBY input switches down all except the +24 V oven supply, the +18 V supply, and the +5 V (L) and (G) supplies.

6.5 TECHNICAL DESCRIPTION

6.5.1 THE RF GENERATING SYSTEM

6.5.1.1 The majority of the circuitry for this system is contained in sealed modules, which should be replaced in the event of a circuit failure. A detailed technical description is given for the audio system assembly, 19-1048, only.

6.5.2 THE AUDIO SYSTEM ASSEMBLY

6.5.2.1 Introduction

6.5.2.1.1 The audio system assembly is mounted on a single printed circuit board, and forms part of the module pack. The purpose of the assembly is to provide the modulating signals for the FM system module and the output system module. The modulating signals may be derived from either of the two audio outputs of the reference generator module or from external sources.

6.5.2.1.2 The general functioning of the system is illustrated in the block diagram, Fig. 6.2. The complete circuit is shown in Fig. 8 in Section 8 of this manual. From the block diagram it will be seen that the system comprises two similar signal processing channels and a control channel.

6.5.2.2 The FM/ØM Channel

6.5.2.2.1 The audio outputs of the reference system module enter assembly 19-1048 at coaxial sockets 21 (1 kHz) and 22 (400 Hz), and are fed directly to the modulating-source-selection circuit. The signal from an external modulation source enters the assembly at SK23, and is fed to the AC/DC coupling selection circuit, IC40a and Q1, shown in Fig. 6.3.

6.5.2.2.2 When AC coupling of an external source is in use, Q1 and IC40a are held in the non-conducting state. The input is AC-coupled via C1 and C2. When DC coupling is in use, Q1 and IC40a are held in the low impedance state. When in the "on" state, Q1 has a lower impedance than IC40a.

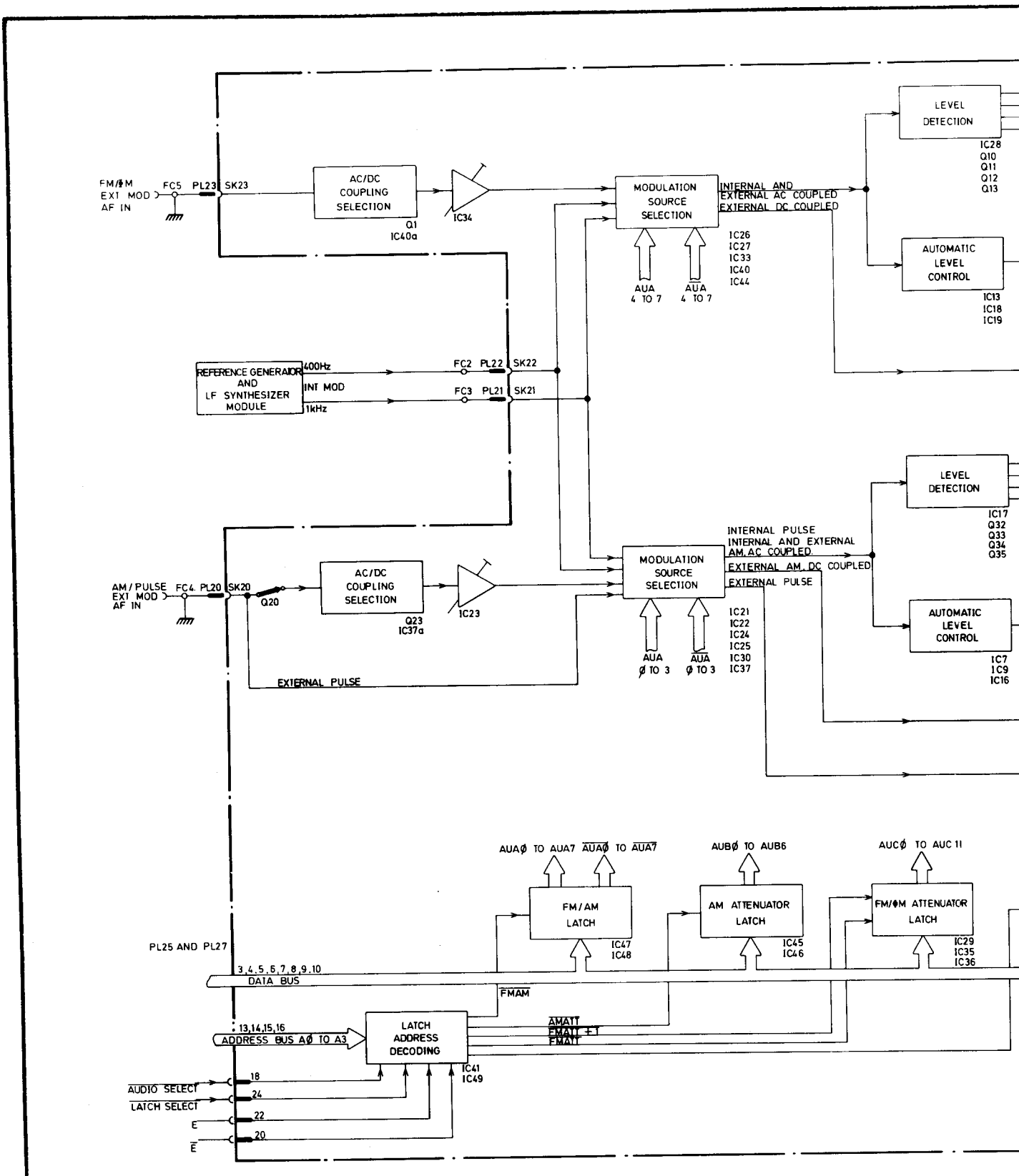
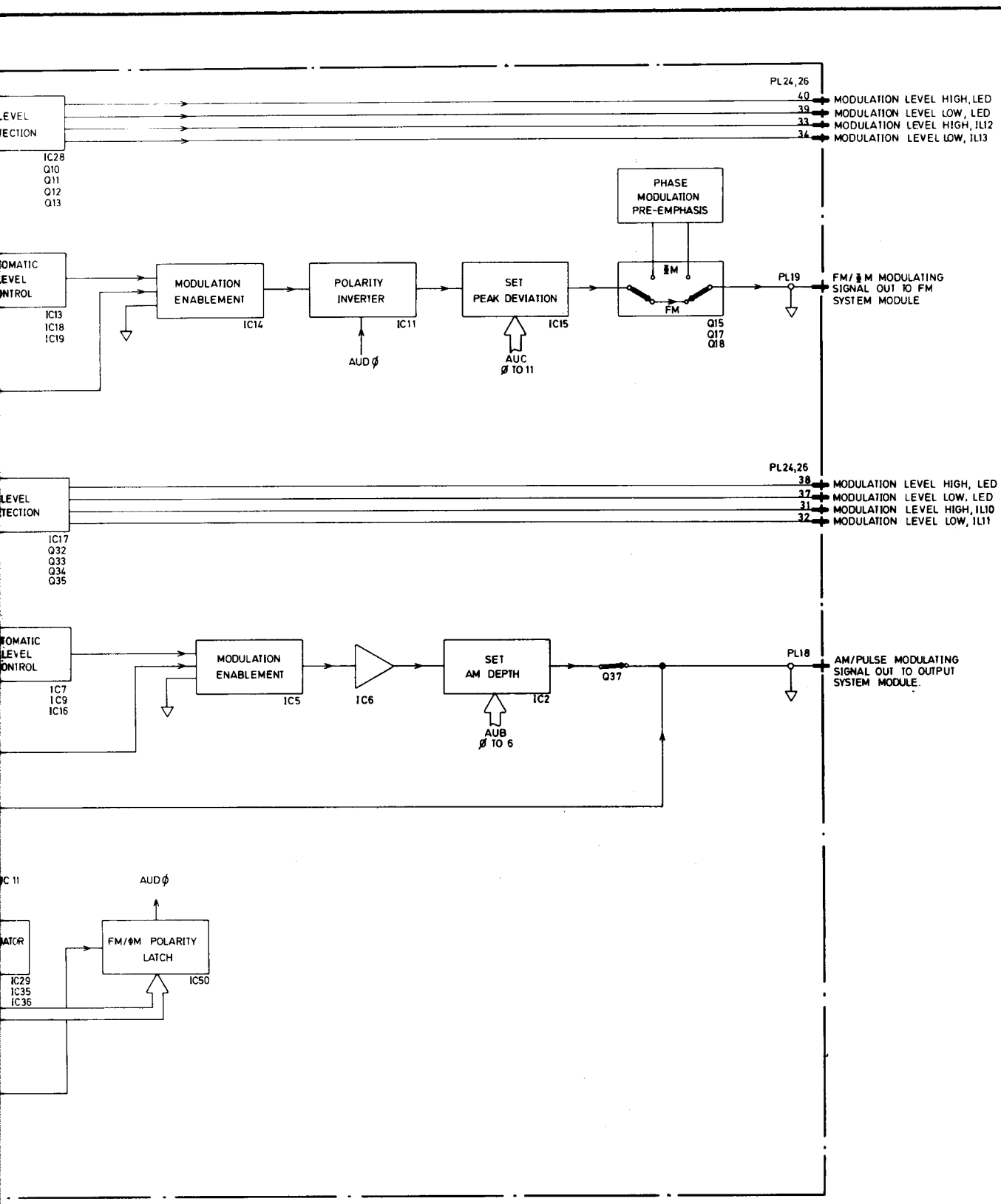


Fig. 6.2. Audio Sys


PL24,26
40
39
33
34
MODULATION LEVEL HIGH, LED
MODULATION LEVEL LOW, LED
MODULATION LEVEL HIGH, IL12
MODULATION LEVEL LOW, IL13
IC28
Q10
Q11
Q12
Q13
PHASE MODULATION PRE-EMPHASIS
MODULATION ENABLEMENT
IC14
POLARITY INVERTER
IC11
SET PEAK DEVIATION
IC15
ØM
FM
Q15
Q17
Q18
PL19
FM/ØM MODULATING SIGNAL OUT TO FM SYSTEM MODULE
IC13
IC18
IC19
AUDØ
AUC Ø TO 11
PL24,26
38
37
31
32
MODULATION LEVEL HIGH, LED
MODULATION LEVEL LOW, LED
MODULATION LEVEL HIGH, IL10
MODULATION LEVEL LOW, IL11
IC17
Q32
Q33
Q34
Q35
MODULATION ENABLEMENT
IC5
IC6
SET AM DEPTH
IC2
Q37
PL18
AM/PULSE MODULATING SIGNAL OUT TO OUTPUT SYSTEM MODULE.
IC7
IC9
IC16
AUB Ø TO 6
AUDØ
FM/ØM POLARITY LATCH
IC50
IC29
IC35
IC36

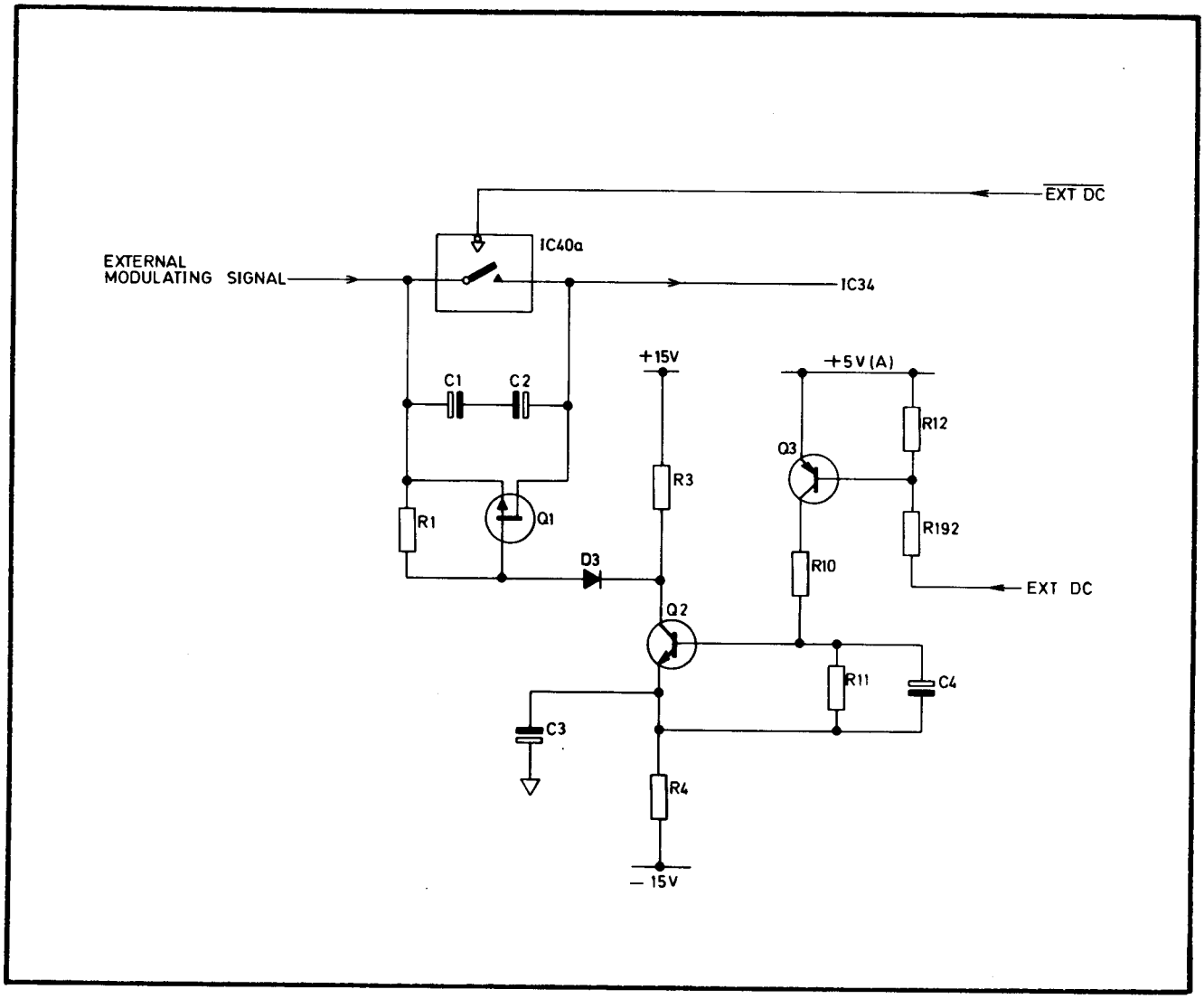


Fig. 6.3 AC/DC Coupling Selection Circuit

6.5.2.2.3 When the circuit is switched to the DC coupling state, it is arranged that the switching signal for Q1, derived via Q2 and Q3, is delayed by C4. This ensures that IC40a goes to the low impedance state first, and prevents the current pulse which occurs if C1 or C2 has become charged from damaging Q1.

6.5.2.2.4 The signal from the coupling selection circuit is amplified by IC34 before being fed to the modulation source-selection-circuit. The gain of the amplifier is adjusted by means of R18, and the amplifier input offset is nulled by means of R17.

6.5.2.2.5 The modulation-source-selection circuit contains 12 bilateral switches. These are arranged in four sets of three, and allow selection of:

(a) 400 Hz internal source
(b) External source, AC-coupled
(c) 1 kHz internal source
(d) External source, DC-coupled

6.5.2.2.6 The logic levels applied to the system with different modulation sources selected and modulation enabled are shown in Table 6.1.

TABLE 6.1

Logic Levels, FM/ØM Modulation Source Selection

Pin	400 Hz INT	EXT AC	1 kHz INT	EXT DC
IC32a/1	1	1	0	0
IC32a/2	1	0	0	1
IC32b/5	1	1	0	0
IC32b/6	0	1	1	0
IC32c/8	0	0	1	1
IC32c/9	0	1	1	0
IC38b/5	0	0	0	0
IC38b/6	1	1	1	0

6.5.2.2.7 When a DC-coupled, external modulating source is selected, the output of the modulation-source-selection circuit is passed direct to the modulation enablement circuit. All other modulating signals, when selected, are fed to the automatic level control (ALC) circuit and the level detector in parallel.

6.5.2.2.8 The ALC circuit is illustrated in Fig. 6.4. In contains a variable attenuator, formed by R32 and Q5, followed by a two-stage fixed-gain amplifier. The impedance of Q5 is varied by feedback from the amplifier output to control the attenuation.

6.5.2.2.9 The feedback path consists of a voltage follower, IC18b; a negative peak detector formed by D10, C28 and R53; a temperature compensation circuit, IC13b; and an integrator, IC13a. The system operates to maintain the input to the integrator at IC13a/6 equal to the reference voltage applied at IC13a/5. This voltage, which is derived across D12, can be adjusted be means of R63 to set the level of the circuit output.

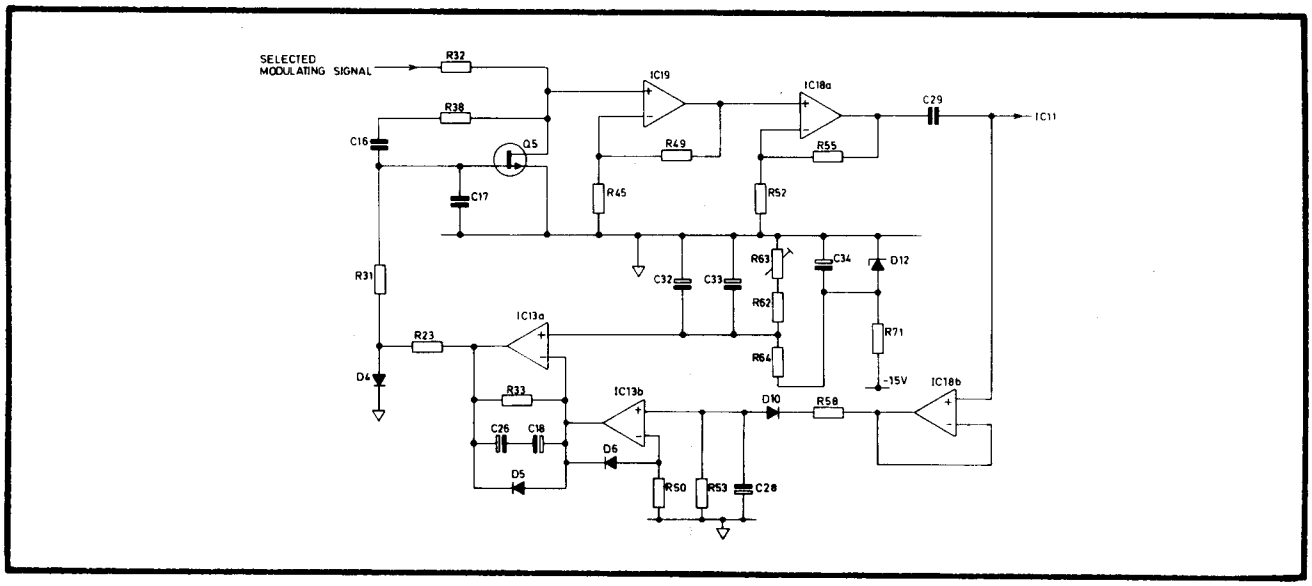


Fig. 6.4 ALC Circuit

6.5.2.2.10 The level detector circuit samples the modulating signal applied to the ALC circuit. It provides both microprocessor interrupt signals and LED indicator drive voltages if the signal level is outside the ALC range.

6.5.2.2.11 The signal applied to the ALC circuit is rectified by D20, C12 and R22. The rectifier output is compared with the voltage levels set by R35 and R36 by the comparators IC28b and IC28a. The levels at IC20c/8 and IC20b/5 are normally at logic '1', but if the modulating signal is out-of-range, one or other input will go to logic '0'. Transistors Q10 and Q11 or Q12 and Q13 will be switched off, and the corresponding interrupt and indicator lines will be pulled up to +5 V.

6.5.2.2.12 When an external source is used with direct coupling, IC20c/9 and IC20b/6 are held at logic '1'. This inhibits the generation of both interrupt and indicator drive signals.

6.5.2.2.13 When the selected form of modulation is disabled, IC20a/1 and IC20d/13 are held at logic '1'. This inhibits the generation of interrupt signals, but not the functioning of the indicators.

6.5.2.2.14 The enablement and disablement of the modulation is achieved by switching the signal line carrying the selected modulating signal. The circuit elements used and the source of the control signals are shown in Table 6.2.

TABLE 6.2

Modulation Enablement and Disablement, FM/ØM

Modulation Source	Switching Signal Applied at	Modulation Disabled Level	Source of Control Signal
400 Hz INT 1 kHz INT EXT AC	IC14a/1 IC14b/8	'0' '1'	$\overline{\text{AUA6}}$ $\overline{\text{AUA4}}$ and $\overline{\text{AUA5}}$ via IC32d, IC39a and IC8a
EXT DC	IC38b/5	'1'	AUA6

6.5.2.2.15 The action of IC14a and IC14b is to disconnect the output of the ALC circuit and connect the modulation signal line to 0 V. When IC38b/5 is held at logic '1', the selection of the DC-coupled modulation source is inhibited.

6.5.2.2.16 The output of the modulation enablement circuit is fed via a voltage follower, IC11b, to a polarity inverter, IC11a. This circuit is necessary because of the method of operation of the RF synthesizer. At certain frequencies the output of the phase-locked loop in which the modulation is introduced is subtracted, instead of added, in the FM system module. If the polarity of the modulating signal were not reversed at the changeover points, a change of sign of the instantaneous deviation would occur.

6.5.2.2.17 The inverter is controlled by line AUDØ, from the latch IC50. When this line holds IC14d/16 at logic '0', IC11/3 is held at 0 V. In this condition, IC11 has a gain of -1, which can be accurately set by means of R57.

6.5.2.2.18 When IC14d/16 is held at logic '1', IC11/3 is fed with the output voltage of the ALC circuit, via R59. In this condition, the gain of IC11 is +1, giving the required signal inversion.

6.5.2.2.19 The signal from the inverter is scaled, to provide control of the peak deviation, in the programmable attenuator, IC15. The attenuation is set according to the logic levels held on control lines AUCØ to AUC 11 by the latches IC29, IC35, and IC36. All the control lines are at logic '0' for minimum peak deviation (maximum attenuation). The peak deviation is variable in 3000 steps according to the binary number set by the control lines on IC15/4 to 15 (IC15/15 carries the least significant bit).

6.5.2.2.20 The attenuator output is buffered in IC12. The input offset of this device can be nulled by adjustment of R78.

6.5.2.2.21 When FM is in use, the output of IC12 forms the modulating signal fed to the FM system module. When phase modulation is in use, the modulating signal must be preemphasized so that a constant amplitude of modulating signal provides a constant peak phase deviation at all modulation frequencies. The preemphasis is achieved by diverting the modulating signal through a filter circuit when phase modulation is in use.

6.5.2.2.22 When FM is selected, control line AUA 7 is at logic '1'. This switches off Q19, thus switching Q16 off and Q14 on. As a result Q17 conducts, while Q15 and Q18 are in the high impedance state. When phase modulation is selected, the states of Q15, Q17 and Q18 are reversed. The modulating signal is then fed to the passive high-pass filter formed by C42 and R81.

6.5.2.2.23 The output of the filter, which increases with modulating frequency, is amplified in IC8. The gain of the amplifier is set by adjustment of R82 so that the modulating signal has the required rate of increase with modulating frequency.

6.5.2.2.24 Above the upper limit of modulating frequency, the gain of IC8 is reduced due to the frequency selective feedback provided by C45 and R94. This reduces the effects of noise in the system. The input offset of IC8 is nulled by adjustment of R89.

6.5.2.3 The AM/Pulse Modulation Channel

6.5.2.3.1 The operation of the AM/Pulse Modulation channel is essentially the same as that of the FM/ØM channel described in paragraph 6.5.2.2. The following paragraphs give information regarding the differences between the channels only.

6.5.2.3.2 When pulse modulation using an external source is selected, the modulating signal bypasses the AC/DC-coupling-selection circuit, and is fed directly to the modulation source selection circuit. When pulse modulation is selected, control line AUA3 is at logic '0'. This turns on Q22 and Q21, putting Q20 to the high impedance state.

6.5.2.3.3 The modulation-source-selection circuit contains 15 bilateral switches, These are arranged in five sets of three, and allow selection of

(a) 400 Hz internal source for AM or pulse modulation
(b) External source, AC-coupled for AM
(c) 1 kHz internal source for AM or pulse modulation
(d) External source, DC-coupled for AM
(e) External source for pulse modulation

6.5.2.3.4 The logic levels applied to the system with different modulation sources selected and enabled are shown in Table 6.3.

TABLE 6.3

Logic Levels, AM/Pulse Modulation Selection

Pin	400 Hz INT		EXT AC		1 kHz INT		EXT DC	
	AM	PULSE	AM	PULSE	AM	PULSE	AM	PULSE
IC43a/1	1	1	0	0	0	0	1	1
IC43a/2	1	1	1	1	0	0	0	0
IC43b/5	1	1	1	1	0	0	0	1
IC43b/6	0	0	1	1	1	1	0	1
IC43c/8	0	0	1	1	1	1	0	0
IC43c/9	0	0	0	0	1	1	1	1
IC38d/12	1	1	1	1	1	1	0	0
IC38d/13	0	1	0	1	0	1	0	1
IC42c/8	1	1	0	0	1	1	1	0
IC42c/9	1	0	1	0	1	0	1	0

6.5.2.3.3 When pulse modulation is in use with an external source, the modulating signal is passed from the modulation-source-selection circuit direct to the output of assembly 19-1048 at SK18. Under these conditions, Q37 is put to the high impedance state by a logic '0' level applied at the base of Q36. When AM is in use with an external source and DC coupling, the modulating signal is passed from the modulation-source-selection circuit to the modulation enablement circuit. In all other cases the modulating signal is fed to an ALC circuit and a level detector circuit similar to those in the FM/ØM channel.

6.5.2.3.4 In the level detector circuit, the generation of both LED indicator drive signals and microprocessor interrupts is inhibited, by a logic '1' level at IC10c/9 and IC10d/12, when either pulse modulation or a DC-coupled external modulating source is selected. Inhibition of interrupt generation also occurs when the modulation is disabled, due to a logic '1' level applied at IC10a/1 and IC10b/5.

6.5.2.3.5 The enablement and disablement of pulse modulation using an external source is carried out in the output system module, 19-1044. The circuit elements used and the source of the control signals for other modulating sources is shown in Table 6.4.

TABLE 6.4

Modulation Enablement and Disablement, AM and Pulse Modulation

Modulation Source	Switching Signal Applied at	Modulation Disabled Level	Source of Control Signal
400 Hz INT 1 kHz INT EXT AC (AM)	IC5a/1 IC5b/14	'1' '0'	See Fig 6.5 $\overline{\text{AUA2}}$
EXT DC (AM)	IC38d/13	'1'	AUA2 and $\overline{\text{AUA3}}$ IC42d

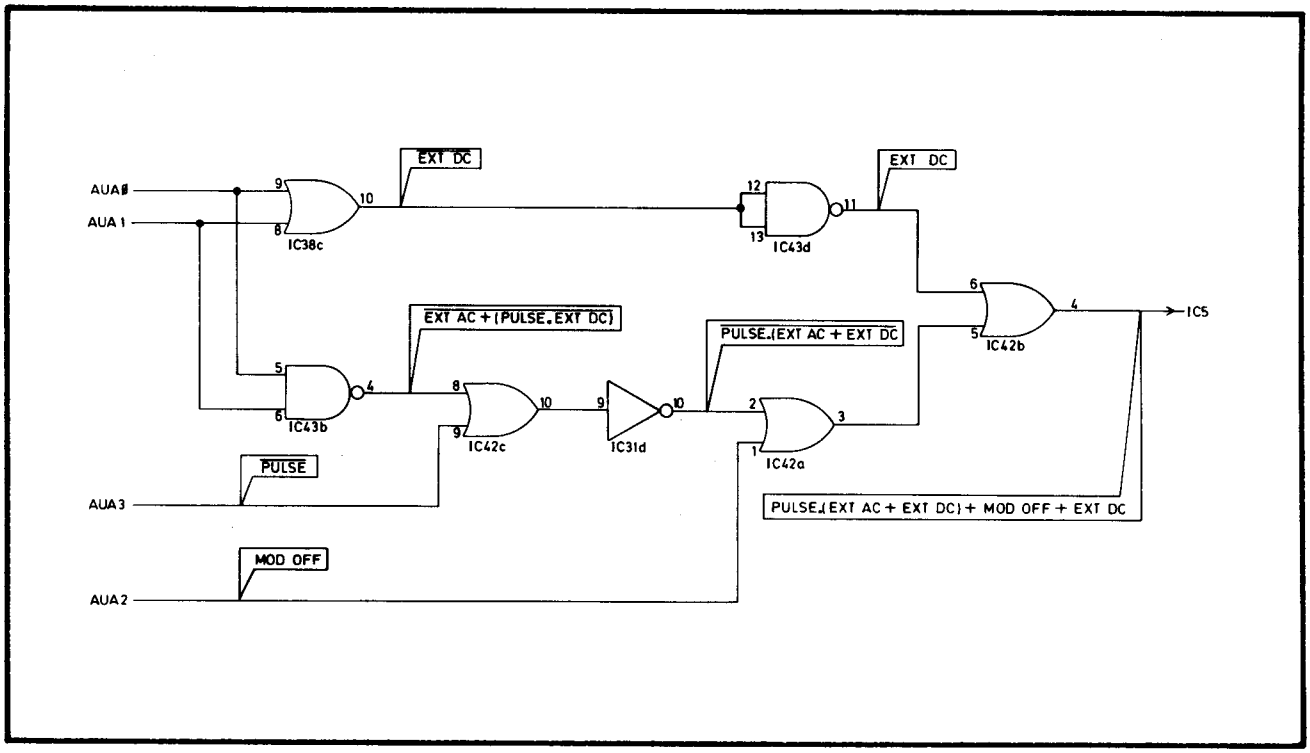


Fig. 6.5 Derivation of Modulation Control Signals

6.5.2.3.6 The scaling of the modulating signal to provide control of the AM depth is performed in the programmable attenuator, IC2. Only seven control lines, AUBØ to AUB6, are used. Connection to IC2 is made via the +5 V to +15 V logic-level-transition circuits, IC1 and IC3.

6.5.2.3.7 All the lines are at logic '0' for zero modulation depth. The AM depth is variable in 99 steps according to the binary number set by the control lines on IC2/11 to 4 (IC2/11 carries the least significant bit). When pulse modulation is selected, all the control lines are put to logic '1'.

6.5.2.3.8 No polarity inverting circuit or preemphasis filter is required in this channel.

6.5.2.4 The Control Channel

6.5.2.4.1 The control channel contains the control line latches and the latch-address-decoding circuit. The address decoding circuit is in two parts:

(a) IC41, enabled by the $\overline{\text{AUDIO SELECT}}$ signal, at PL25 and PL27 pin 18, and the microprocessor E signal, at PL25 and PL27 pin 22. This decodes addresses for the FM/AM latch and the two attenuator latches.

(b) IC49, enabled by the $\overline{\text{LATCH SELECT}}$ signal, at PL25 and PL27 pin 24, and the microprocessor $\overline{\text{E}}$ signal, at PL25 and PL27 pin 20. This decodes the address for the FM/ØM polarity latch.

6.5.2.4.2 The polarity latch, IC50, holds control line AUDØ at the level set in at IC50/12 by data line D4 during latch enablement. A logic '1' level sets the gain of IC11 to +1.

6.5.2.4.3 The AM attenuator latch comprises IC45 and IC46. These are enabled simultaneously by the $\overline{\text{AMATT}}$ output from IC41/13, which is applied at IC45/6 and IC46/6, and so form a single eight-bit wide latch. Only seven outputs are used, these being held at the levels set in by data lines DO to D6 during latch enablement.

TABLE 6.5

AUA Control Line Logic Levels

System	Function	Control Lines							
		7	6	5	4	3	2	1	0
AM/PULSE	EXT DC							0	0
	400 Hz INT							0	1
	1 kHz INT							1	0
	EXT AC							1	1
	MOD ON						1		
	MOD OFF						0		
	AM					1			
	PULSE					0			
FM/ØM	EXT DC			0	0				
	400 Hz INT			0	1				
	1 kHz INT			1	0				
	EXT AC			1	1				
	MOD ON		1						
	MOD OFF		0						
	FM	1							
	ØM	0							

6.5.2.4.4 The FM attenuator latch comprises IC29, IC35 and IC36. The latch is addressed in two stages. When the $\overline{\text{FMATT}}$ signal from IC41/15 is applied at IC36/6, control lines AUC 8 to AUC 11 are set to the levels on data lines DO to D3. Next, the $\overline{\text{FMATT+1}}$ signal from IC41/14 is applied to IC29/6 and IC35/6 in parallel, enabling both latches. The outputs are then set to the levels on data lines DO to D7.

6.5.2.4.5 The FM/AM latch comprises IC47 and IC48. These are enabled simultaneously by the $\overline{\text{FMAM}}$ output from IC41/12, and so form a single eight-bit wide latch. The Q outputs are held at the levels set in by data lines DO to D7 during latch enablement.

6.5.2.4.6 The control line logic levels are as shown in Table 6.5.

6.5.3 THE CONTROL, MEMORY, AND DISPLAY SYSTEM

6.5.3.1 The circuitry for this system is mounted on the following assemblies:

(a) Processor assembly, 19-1051
(b) Non-volatile memory assembly, 19-1049
(c) Display assembly, 19-1041
(d) Motherboard assembly, 19-1043
(e) GPIB assembly, 19-1050
(f) Audio system assembly, 19-1048
(g) FM system assembly, 11-1535
(h) Output system assembly, 11-1532
(j) Comb loop assembly, 11-1533

6.5.3.2 The assemblies of the system are interconnected by the instrument data and address buses, and by a number of control lines. A schematic diagram of the main interconnections is given in Fig. 6.6.

6.5.3.3 The system is controlled by a microprocessor, which is mounted on the processor assembly. The microprocessor is interrupt-controlled, using a system of 32 interrupt lines. A schematic diagram of the interrupt line system is given in Fig. 6.7

6.5.4 THE PROCESSOR ASSEMBLY

6.5.4.1 Introduction

6.5.4.1.1 The processor assembly carries the microprocessor, the program ROM, a RAM, part of the address decoding circuitry and the interrupt request generating and polling circuits. A diagram of the bus layout connecting the processor assembly to other assemblies within the instrument is shown in Fig. 6.6, while the interrupt system is shown schematically in Fig. 6.7. The complete circuit of the processor assembly is shown in Fig. 14 in Section 8 of this manual.

6.5.4.2 The Bus Stucture

6.5.4.2.1 The data bus is in two parts. A local data bus is used to connect the microprocessor to the ROM, the RAM, and the interrupt circuitry on the processor assembly. The local bus buffer, IC27, is enabled by IC24 when this bus is in use. At all other times, IC27 is disabled and IC44 is enabled. This connects the microprocessor to the instrument's data bus, which passes off the assembly to the motherboard and the rest of the instrument at PL14.

6.5.4.2.2 The instrument's address bus is driven by the microprocessor, IC26, via the buffers, IC25 and IC35. The bus connects to the address decoders on the assembly, and passes off the assembly to the motherboard and the rest of the instrument at PL14.

6.5.4.3 Control Line Decoding

6.5.4.3.1 The high-order address bits, on lines A11 to A15, are decoded in IC23 or IC45. All addresses having A15 at logic '1' are decoded in IC23, and are used for the program ROM. Addresses with A15 at logic '0' are decoded by IC45 into the control line signals shown in Table 6.6.

6.5.4.3.2 The low-order bits of those addresses for which IC45 holds the INTERFACE SELECT control line at logic '0' are decoded in IC17 to give the local control line signals shown in Table 6.7. Whenever the INTERFACE SELECT line is at logic '0', IC24/9 is at logic '1', IC27 is enabled, and IC44 is disabled. The microprocessor is then connected to the local data bus.

TABLE 6.6

System Control Lines

IC45 pin	NAME	USE
1	$\overline{\text{RAM SELECT}}$	Selects IC13 Selects local data bus.
2	$\overline{\text{INTERFACE SELECT}}$	Enables local control line decoder, IC17 Selects local data bus.
3	$\overline{\text{POWVAL}}$	Address of valid power latch on non-volatile memory assembly.
4	$\overline{\text{AUDIO SELECT}}$	Audio-system assembly latch addressing.
5	$\overline{\text{GPIB SELECT}}$	GPIB interface addressing.
6	$\overline{\text{DISPLAY SELECT}}$	Display system addressing.
7	$\overline{\text{LATCH SELECT}}$	Addressing on audio system assembly, motherboard, comb loop assembly, FM assembly, and output assembly.
8	$\overline{\text{ATTEN SELECT}}$	Output attenuator, LF synthesizer, and auxiliary input addressing.
9, 10	MEM 1	Non-volatile memory addressing
11, 13	MEM 2	

TABLE 6.7

Processor Assembly Local Control Lines

IC17 Pin	Name	Use
1	$\overline{\text{IRQ PL1}}$	Interrupt polling lines
2	$\overline{\text{IRQ PL2}}$	
3	$\overline{\text{IRQ PL3}}$	
4	$\overline{\text{IRQ PL4}}$	
5	$\overline{\text{KBDRD}}$	Keyboard read buffer servicing
6	$\overline{\text{KBDCLR}}$	Clears keyboard $\overline{\text{IRQ}}$ after servicing
7	$\overline{\text{SWRD}}$	Spinwheel read buffer servicing
8	$\overline{\text{SWCLR}}$	Clears spinwheel counter and IRQ after servicing
9	$\overline{\text{KBDWR}}$	Keyboard write buffer servicing
10	$\overline{\text{OPTPOL}}$	Special function poll of options fitted
13	$\overline{\text{SETSBY}}$	Control of standby line
14	$\overline{\text{CLRSBY}}$	

6.5.4.4 The System Clocks

6.5.4.4.1 All activity on the bus is synchronized by the microprocessor's 1 MHz clock signal from IC26/37. Four clock signals are derived from this output. These are designated PROCE, E, $\overline{E}$ and GPIBCLK.

6.5.4.4.2 GPIBCLK is the clock signal for the GPIB interface. It is taken from IC26/37 via a buffer, IC22c, and leaves the assembly at PL14 Pin 8. This clock runs continuously.

6.5.4.4.3 The remaining clock signals are taken from IC26/37 via the buffer IC22a, which is disabled by a logic '1' level from IC26/7 whenever the microprocessor is waiting for an interrupt to occur. As a result these clock signals are present only during periods of bus activity, and a low level of radio frequency interference is obtained.

6.5.4.4.4 The PROCE clock is taken from IC22a/3 and can be monitored at TP9. the signal leaves the assembly at PL14 pin 7.

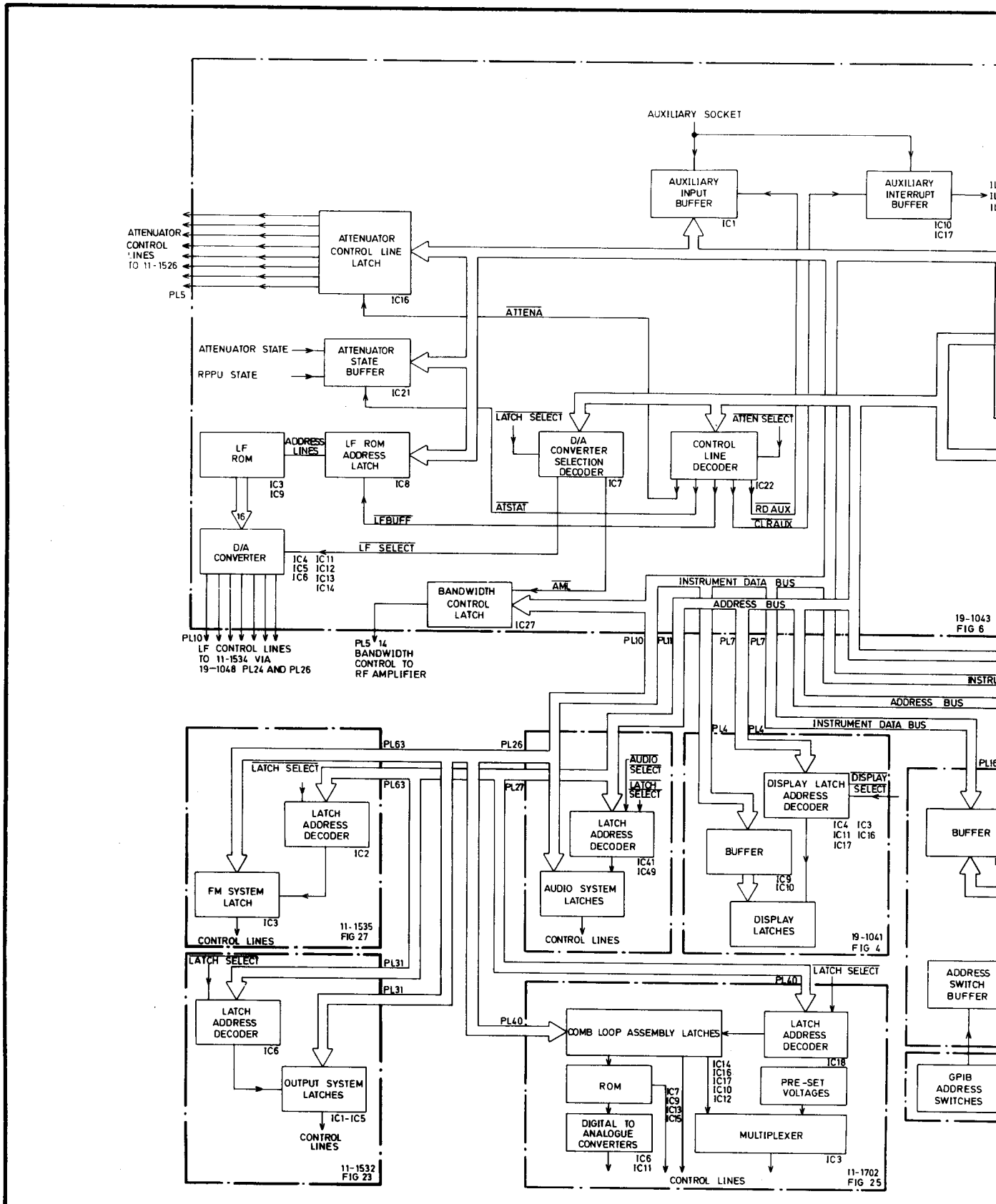
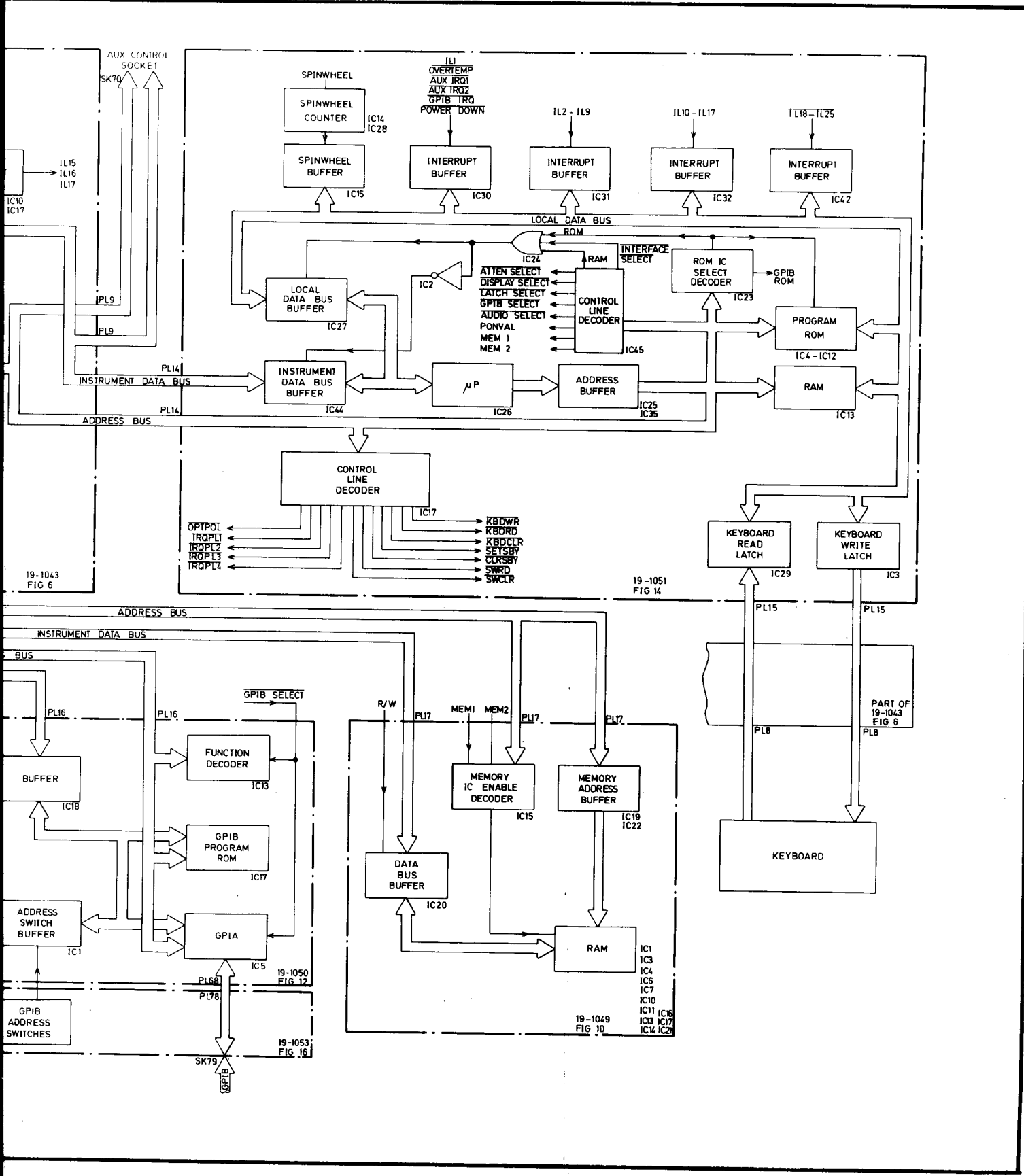

AUXILIARY SOCKET
AUXILIARY INPUT BUFFER
IC1
AUXILIARY INTERRUPT BUFFER
IC10 IC17
ATTENUATOR CONTROL LINES TO 11-1526
PL5
ATTENUATOR CONTROL LINE LATCH
IC16
ATTENA
ATTENUATOR STATE
RPPU STATE
ATTENUATOR STATE BUFFER
IC21
LATCH SELECT
ATTEN SELECT
LF ROM
ADDRESS LINES
LF ROM ADDRESS LATCH
IC3 IC9
IC8
D/A CONVERTER SELECTION DECODER
IC7
CONTROL LINE DECODER
IC22
ATSTAT
RD AUX
CLR AUX
LFBUFF
16
D/A CONVERTER
LF SELECT
IC4 IC11 IC5 IC12 IC6 IC13 IC14
BANDWIDTH CONTROL LATCH
IC27
AM
INSTRUMENT DATA BUS
ADDRESS BUS
19-1043 FIG 6
PL10
LF CONTROL LINES TO 11-1534 VIA 19-1048 PL24 AND PL26
PL5 14
BANDWIDTH CONTROL TO RF AMPLIFIER
PL63
PL26
PL4
LATCH SELECT
LATCH ADDRESS DECODER
IC2
FM SYSTEM LATCH
IC3
CONTROL LINES
11-1535 FIG 27
AUDIO SELECT
LATCH SELECT
PL27
LATCH ADDRESS DECODER
IC41 IC49
AUDIO SYSTEM LATCHES
CONTROL LINES
DISPLAY LATCH ADDRESS DECODER
DISPLAY SELECT
IC4 IC3 IC11 IC16 IC17
BUFFER
IC9 IC10
DISPLAY LATCHES
19-1041 FIG 4
BUFFER
PL31
LATCH ADDRESS DECODER
IC6
OUTPUT SYSTEM LATCHES
IC1-IC5
CONTROL LINES
11-1532 FIG 23
PL40
COMB LOOP ASSEMBLY LATCHES
LATCH ADDRESS DECODER
IC18
ROM
IC7 IC9 IC13 IC15
IC14 IC16 IC17 IC10 IC12
PRE-SET VOLTAGES
DIGITAL TO ANALOGUE CONVERTERS
IC6 IC11
MULTIPLEXER
IC3
CONTROL LINES
11-1702 FIG 25
ADDRESS SWITCH BUFFER
GPIB ADDRESS SWITCHES

Fig. 6.6 Bu



6.6 Bus Structure

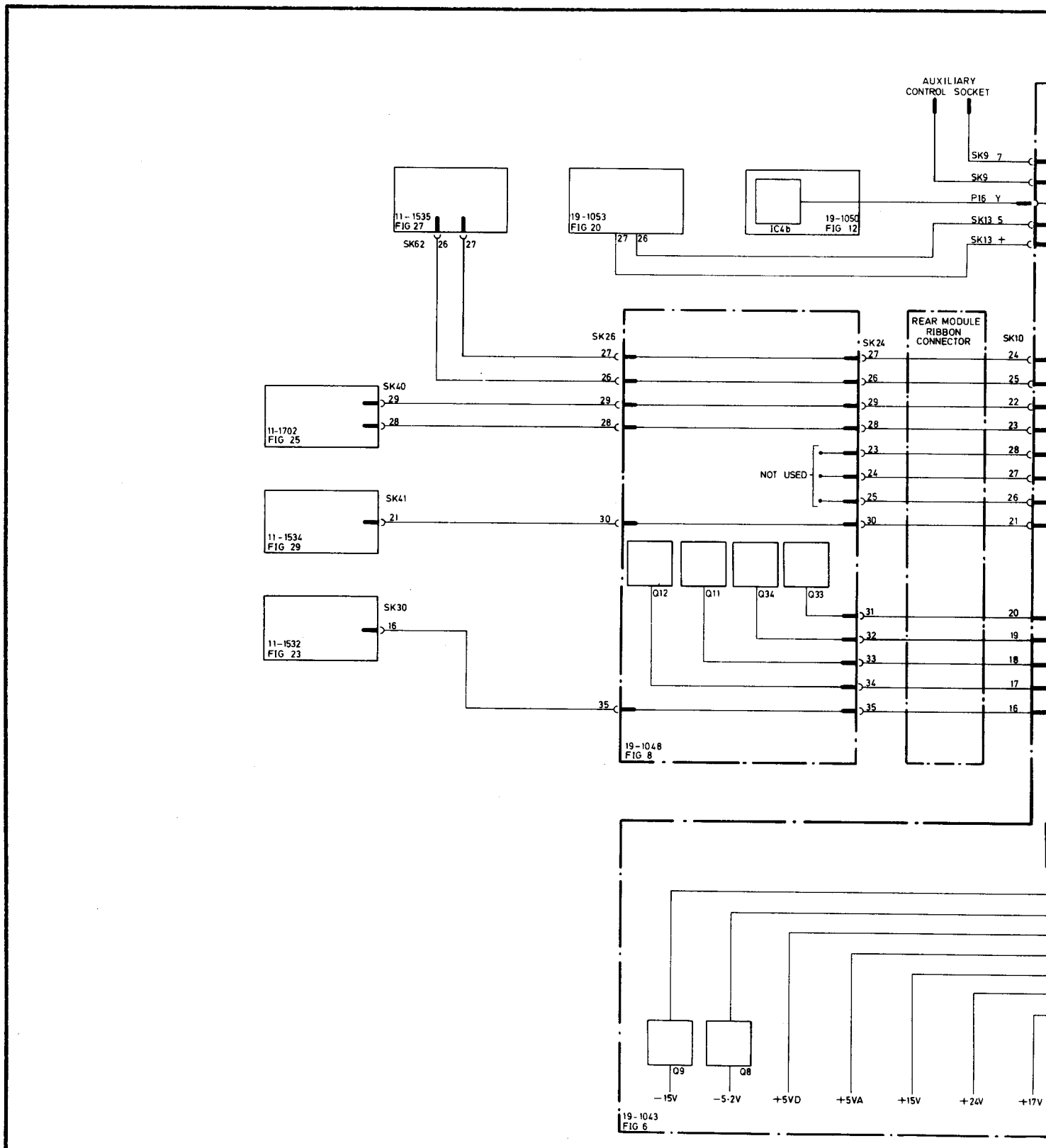
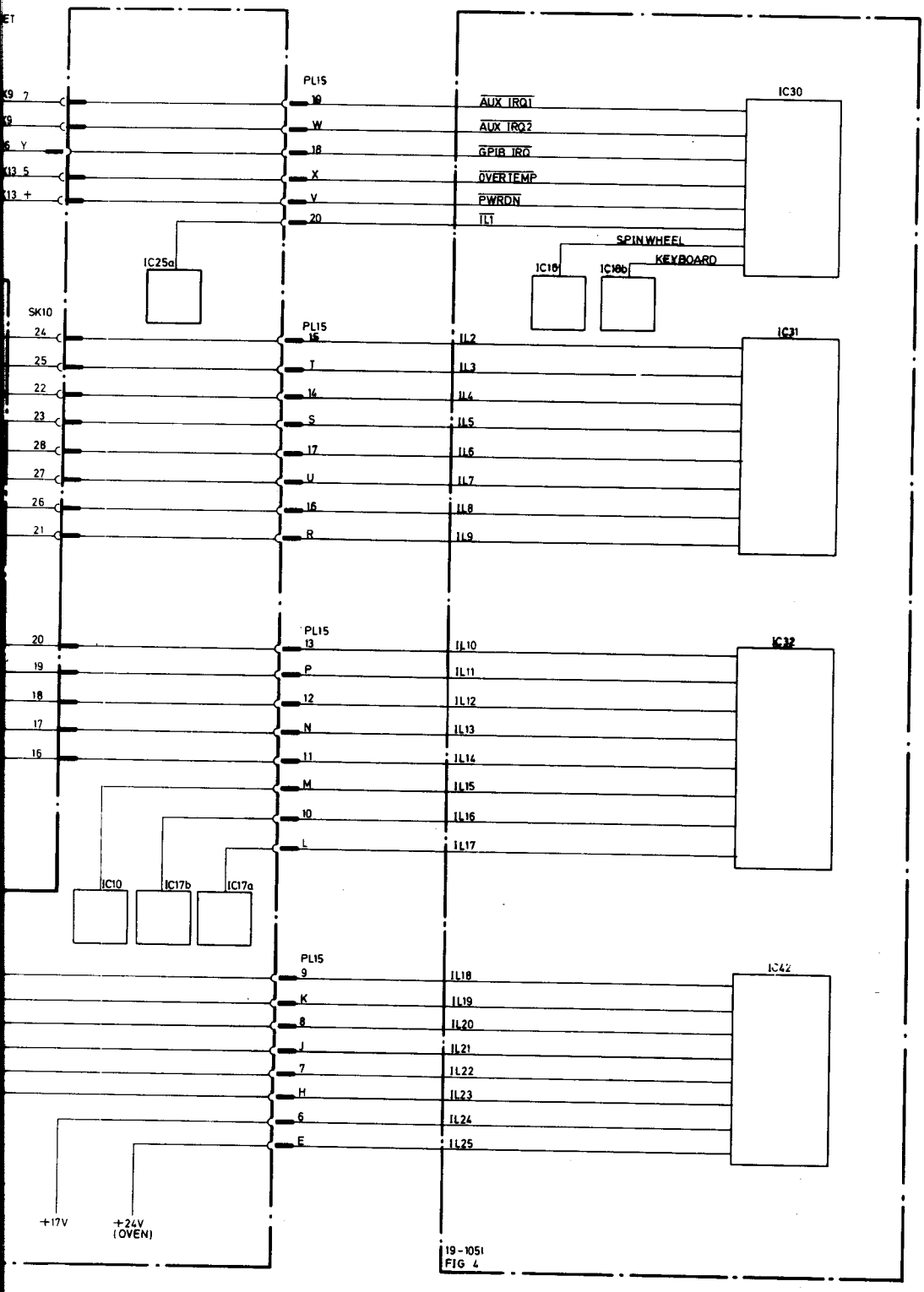


Fig. 6.7 Interrup



errupt System

6.5.4.4.5 The E and $\overline{E}$ clocks are derived from the PROCE clock in the circuit containing IC19a, IC34a, b and c, and IC36a, shown in Fig. 6.8. When the microprocessor is reading data from the bus, E and $\overline{E}$ are a copy and the inverse of PROCE. During microprocessor write operations, however, E and $\overline{E}$ are modified to increase the time during which valid data may be read from the bus.

6.5.4.4.6 During microprocessor read operations, IC36a/3, and therefore IC34c/10, are put to logic '0' by the R/$\overline{W}$ line from IC26/34. This gives a logic '1' level at IC34b/4, so that the $\overline{E}$ clock appearing at IC34b/6 is the inverse of the PROCE signal applied at IC34b/5. The E clock is derived from $\overline{E}$ in IC34a.

6.5.4.4.7 During microprocessor write operations, IC34c/10 is held at logic '1', and the level at IC34b/4 is governed by the $\overline{Q}$ output of the monostable circuit, IC19a. The operation of the circuit is illustrated in Fig. 6.9. It can be seen that the active (positive-going) edge of the $\overline{E}$ waveform now occurs before the active (negative-going) edge of PROCE, and the data hold-time, for which valid data can be read from the bus, is increased.

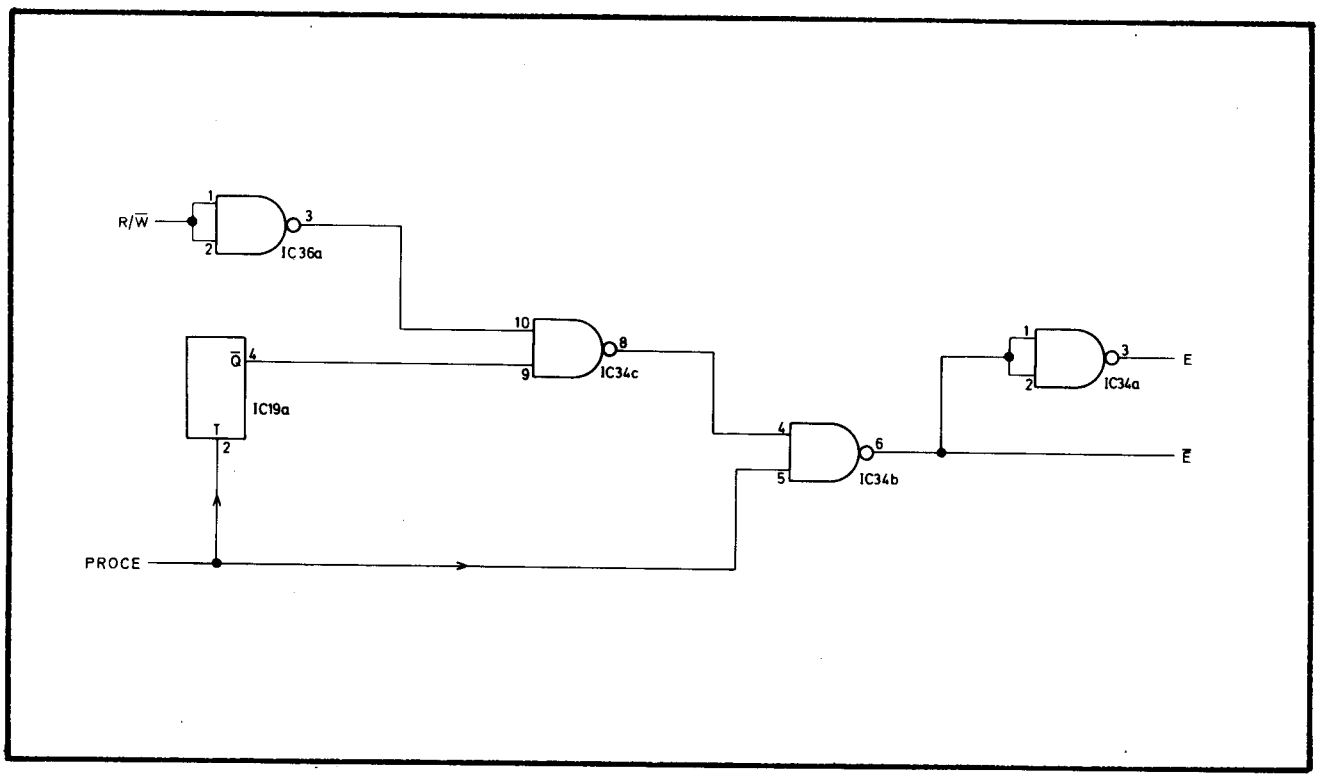


Fig 6.8 Timing Modification Circuit

6.5.4.5 Addressing the Program ROM

6.5.4.5.1 The ROM ICs are addressed in parallel using address lines A0 to A10. The required IC is selected by an output from IC23, decoded from the high order bits of the address "on" lines A11 to A15 and a $\overline{VMA}$ signal derived from IC26/5. When any of IC4 to IC12 is selected, one input of IC24 goes to logic '0'. The resulting logic '1' at IC24/9 enables the local data bus buffer, IC27, and disables IC44. The data transfer to the local data bus is made when the ROM output is enabled by the $\overline{E}$ clock.

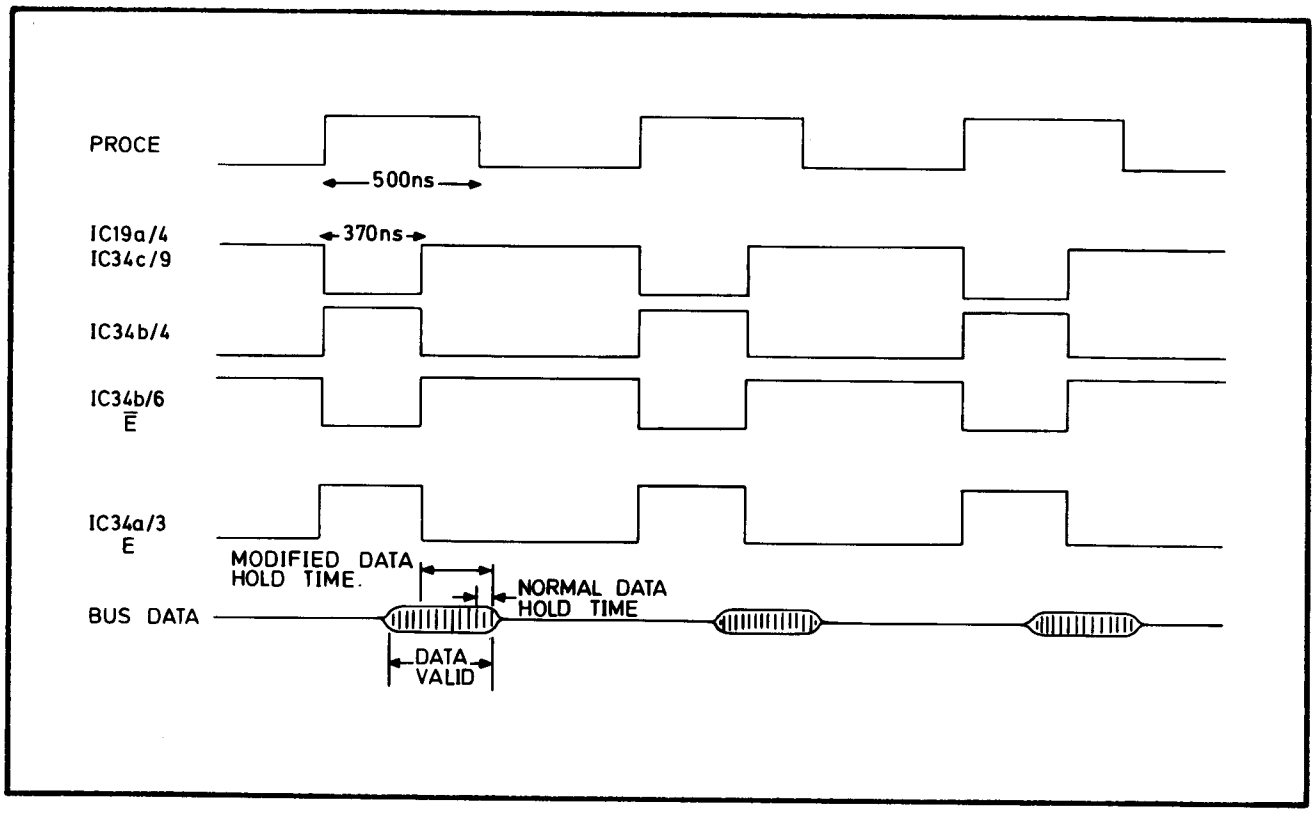


Fig. 6.9 Timing Modification Waveforms - Write Operation

6.5.4.6 The Random Access Memory

6.5.4.6.1 The RAM, IC13, is addressed using lines A0 to A9 and selected by the $\overline{\text{RAM SELECT}}$ output from IC45. The $\overline{\text{RAM SELECT}}$ signal is applied to one input of IC24. This enables IC27 and disables IC44, connecting the microprocessor to the local data bus.

6.5.4.6.2 During microprocessor read operations, the R/$\overline{\text{W}}$ line holds IC34d/13 at logic '1'. Data transfer to the bus occurs when the RAM output is enabled by the inverted PROCE clock at IC13/20. During microprocessor write operations, IC36a/3 is at logic '1', and the $\overline{\text{E}}$ clock signal is applied to the write enable input, IC13/21. Data transfer from the bus occurs when this input is in the logic '0' state.

6.5.4.7 Interrupt Operation

6.5.4.7.1 The 32 interrupt lines are connected to the buffers and line drivers IC30, IC31, IC32 and IC42. A schematic diagram of the interrupt line system is given in Fig. 6.7. At the connections to IC30, the interrupt condition is represented by a logic '0', and an inverting buffer is used. At the connections to IC31, IC32, and IC42, the interrupt condition is represented by a logic '1'.

6.5.4.7.2 When an interrupt occurs, an interrupt request ($\overline{\text{IRQ}}$) is generated in IC38, IC39, IC40 or IC43, and is fed to the microprocessor at IC26/4 via the test switch, S2. The microprocessor enters its interrupt routine, and carries out a poll of IC30, IC31, IC32, and IC42 to establish the cause of the interrupt.

6.5.4.7.3 The poll procedure is as follows:

(a) The microprocessor addresses IC30 ($\overline{\text{IRQ PL1}}$)

(b) The high order address bits are decoded in IC45, and IC45/2 ($\overline{\text{INTERFACE SELECT}}$) goes to logic '0'.

(c) The $\overline{\text{INTERFACE SELECT}}$ signal at IC24/4 puts IC24/9 to logic '1'. This enables IC27 and disables IC44, connecting the microprocessor to the local data bus.

(d) IC17 is enabled by the $\overline{\text{INTERFACE SELECT}}$ and $\overline{\text{E}}$ signals. It decodes the address bits on lines A0 to A3, and IC17/1 ($\overline{\text{IRQ PL1}}$) goes to logic '0'. As a result IC30 is enabled, and the microprocessor reads the interrupt line settings.

(e) The process is repeated in respect of IC31, IC32, and IC42 until the cause of the interrupt is known.

6.5.4.8 Keyboard Operation

6.5.4.8.1 The keys are connected on an eight-by-eight matrix. The rows are connected to the outputs of IC1 and IC2 via the keyboard address bus, while the columns are connected to the inputs of IC29 by the keyboard data bus. The keyboard data bus is normally pulled up to a logic '1' level by R23, while the keyboard address bus lines are held at logic '0' by IC1 and IC2.

6.5.4.8.2 If any key is operated, the corresponding lines of the address and data buses are connected, and the data bus line is pulled to logic '0'. When this happens IC37/8 goes to logic '1', and IC18b is clocked to the set state via IC20d and f. The logic '0' at IC18/8 ($\overline{\text{KBD IRQ}}$) generates a microprocessor $\overline{\text{IRQ}}$ via IC38a.

6.5.4.8.3 Once the keyboard has been identified as the cause of the interrupt by the interrupt polling routine, the microprocessor services the keyboard to locate the key which has been operated. The microprocessor addresses IC3 ($\overline{\text{KBDWR}}$) and sets one line of the keyboard address bus to logic '0'. The microprocessor then addresses IC29 ($\overline{\text{KBDRD}}$) and reads the keyboard data bus. These operations are repeated until the operated key is located.

6.5.4.8.4 If the operated key is in the row set to logic '0' by the address bus a logic '0' will appear on the data bus. The position of this logic '0' on the bus indicates the position of the key within the row. Thus each key is associated with a different combination of keyboard address and keyboard data byte, and can be individually identified.

6.5.4.8.5 When the operated key has been identified, the microprocessor resets the keyboard interrupt by addressing $\overline{\text{KBDCLR}}$. This resets IC18b.

6.5.4.9 Spinwheel Operation

6.5.4.9.1 When the spinwheel is operated, two streams of pulses are generated on the display assembly, 19-1041. The pulse generators are of the optically-coupled type. Light from a LED is reflected by a disc attached to the spinwheel to a phototransistor. This disc has radial strips of high and low reflectance, so the optical coupling is varied as the disc rotates. The two pulse generators are positioned so that the two pulse streams are 90° out-of-phase.

6.5.4.9.2 The two pulse streams enter the processor assembly at PL15, pins Z and 23, and are applied to a counter formed by IC14 and IC28 in cascade. For one direction of spinwheel rotation, one waveform will hold IC14/10 at logic '1' when the second waveform clocks IC14/15, and the counter will count up. For the other direction of spinwheel rotation, IC14/10 is at logic '0' when clocking occurs, giving a down count.

6.5.4.9.2 As soon as an output occurs from IC14 or IC28, a logic '0' level occurs at IC30/2, and a microprocessor $\overline{IRQ}$ is generated via IC38a. Once the spinwheel has been identified as the cause of the interrupt by the interrupt polling routine, the microprocessor services the spinwheel. This is done by addressing IC15 ($\overline{SWRD}$) and reading the spinwheel counter output. Changes in the counter output during reading are prevented by holding IC14/5 and IC28/5 at logic '1' via IC21b, so disabling the counter.

6.5.4.9.3 After the counter has been read the microprocessor addresses $\overline{SWCLR}$. This resets the counter and clears the spinwheel interrupt.

6.5.4.10 Reset Circuit

6.5.4.10.1 When the instrument is switched on, the reset circuit, containing Q1, Q2, and Q3 holds IC20e/11 below its trigger level until C10 charges. This holds IC26/40 low, providing the microprocessor $\overline{RESET}$ input. The same signal is fed to the GPIB assembly, 19-1050, to reset the GPIA circuit and to the non-volatile memory assembly, 19-1049, to reset the latches in the battery changeover and charging circuits.

6.5.4.10.2 In the event of a reduction of the +5 V (L) rail voltage, due to power failure or to the instrument being switched off, Q1 conducts. The resulting current in R5 switches on Q3, which draws current from C10 through R7. The voltage drop across R7 switches on Q2, maintaining current through R5, so that Q3 and Q2 remain latched-on even if power is quickly restored. As a result C10 is completely discharged, ensuring a correct reset.

6.5.4.11 Test Switch

6.5.4.11.1 The switch S2 permits the overriding of certain microprocessor-controlled instructions for test purposes. When the instrument is in normal operation, sections a, b and f must be in the closed position, where the slider is towards the top of the board.

6.5.5 THE NON-VOLATILE MEMORY ASSEMBLY

6.5.5.1 Introduction

6.5.5.1.1 The non-volatile memory is used to store complete front-panel settings. It is mounted on a single printed circuit board, which also carries the NiCd, data-maintaining battery and the battery-charging control circuit. The circuit diagram is shown in Fig. 10 in Section 8 of this manual.

6.5.5.1.2 Two sizes of memory are available. The 33 location memory uses IC1, IC3, IC4, and IC7 only. If the additional ICs to increase the number of memory locations to 100 are fitted, LK1, between pins X and 19 of PL17, must also be fitted.

6.5.5.2 Memory Addressing

6.5.5.2.1 The RAM ICs are addressed in pairs via the buffers IC19, IC22a and IC22b, using address lines A0 to A9. The required ICs are selected by an output from IC15, decoded from address lines A10 and A11, and the control lines MEM1 and MEM2. The control lines signals are decoded on the processor assembly from address lines A11 to A15.

6.5.5.2.2 If the memory is not being addressed, both MEM1 and MEM2 are at logic '0', and IC15/12 is held at logic '1' via IC18c, IC18b, and IC8f. In this condition IC15 can only select its unused outputs, numbered 8 or above. The logic '1' from IC8f/12 is also used to disable the data bus buffer, IC20.

6.5.5.3 Read/Write Control

6.5.5.3.1 Read/Write control is exercised by the microprocessor R/$\overline{W}$ line via the buffer, IC22c, and the protection circuit, Q1. The R/$\overline{W}$ line is also connected directly to the data bus buffer, IC20, to control the direction of data transmission.

6.5.5.4 Memory Supply Changeover

6.5.5.4.1 During the microprocessor start-up routine, the valid power latch, IC5a, is addressed. The address is decoded on the processor assembly to provide a logic '0' level on the $\overline{POWVAL}$ line. Data line D0 is put to logic '1' by the microprocessor, and IC5a is clocked to the set state by the PROCE clock.

6.5.5.4.2 With IC5a in the set condition the logic '0' at IC5a/6 enables the address and read/write buffers, IC19 and IC22. The logic '1' at IC5a/5 charges C12 via R8, switching Q4 and Q3 to the conducting state. The memory supply is then provided from the +5 V (L) rail, and a trickle charge is given to the battery via R14.

6.5.5.4.3 If the power failure interrupt occurs, the microprocessor stores the current instrument settings. It then addresses $\overline{POWVAL}$ and sets data line D0 to logic '0', so that IC5a is clocked to the clear state. The logic '1' at IC5a/b then disables IC19 and IC22a, b and c, and gives a logic '1' at IC15/12 and IC20/19. In this way the memory is isolated from both the address and data buses, and cannot be inadvertently addressed by random signals occurring as the power fades.

6.5.5.4.4 The logic '0' at IC5a/5 cuts off Q1 and open-circuits the R/$\overline{W}$ line. The memory end of the line is pulled to logic '1' by R6, holding the memory in the read state.

6.5.5.4.5 The logic '0' at IC5a/5 discharges C12 via D1, and Q4 is cut off. This cuts off Q3, and the memory supply is provided by the battery through R14.

6.5.5.5 The Battery Charging System

6.5.5.5.1 The state of charge of the battery is indicated by its terminal voltage. This voltage is applied to the resistor chain, R16, R17, R18 via PL17 pins 22 and Z (connected on the motherboard assembly). The voltage at the wiper of R17 is compared with an internal reference in the voltage detector IC9.

6.5.5.5.2 If the input to IC9 falls below the reference level, IC9/4 goes to logic '0', putting IC5b to the set state by providing a logic '0' at IC5b/10. The logic '0' at IC5b/8 releases the counter, IC2, from the reset state and switches Q5 on. The battery receives full charging current from the +5 V (L) rail via R13 and D3. The logic '1' at IC5a/9 releases the clock, IC23, from the held state and provides a drive signal to the BATTERY LOW indicator on the display.

6.5.5.5.3 The pulses from IC23/3 are counted in IC2 until IC2/1 goes to logic '0'. This takes approximately 14 hours. The output from IC2/1 clocks IC5b to the reset state, terminating the full-charge cycle.

6.5.5.5.4 The battery charging cycle can be started, if required, by means of a special function. When the special function is enabled, the microprocessor sets the address bus to put IC15/9 to logic '0'. This sets IC5b, via IC12b and IC8c, to start the charge cycle.

6.5.6 THE DISPLAY SYSTEM

6.5.6.1 Introduction

6.5.6.1.1 All the display elements are mounted on one printed circuit board, and are viewed through apertures in the front panel. For each change of displayed information, the complete display, not only the changed element, is rewritten. The circuit diagram is shown in Fig. 4 in Section 8 of this manual.

6.5.6.2 Display Element Addressing

6.5.6.2.1 Each numeric indicator has a separate address. The indicators incorporate latched data stores and the circuitry required to decode the data into the display pattern.

6.5.6.2.2 The LEDs of the external-modulation signal-level indicators are driven by signals derived on the audio system assembly, 19-1048, and the BATTERY LOW indicator LEDs are driven by a signal from the non-volatile memory assembly, 19-1049. The remainder of the LED indicators are grouped, each group being controlled by an addressable latch.

6.5.6.2.3 The low-order address bits, on lines A0 to A3 are fed to the three decoders, IC4, IC11 and IC17. The required decoder is enabled by a logic '0' output from IC16, which decodes the address on lines A4, A5 and DISPLAY SELECT. The DISPLAY SELECT signal is derived on the processor assembly, 19-1051, from address lines A11 to A15.

6.5.6.2.4 On switching to standby, IC19b/14 goes to logic '0' due to the voltage reduction on the +5 V (D) rail. This isolates address lines A0 to A3 from IC4 and IC17. The lines remain connected to IC11, as the STANDBY indicator and GPIB LEDs are required to remain operative.

6.5.6.3 LED Flashing Circuit

6.5.6.3.1 The ERROR indicator, and the STANDBY and EXECUTE key indicators, are required to flash under certain conditions. The flash rate is determined by the circuit containing IC23a and b. The indicator control circuit is shown in Fig. 6.10.

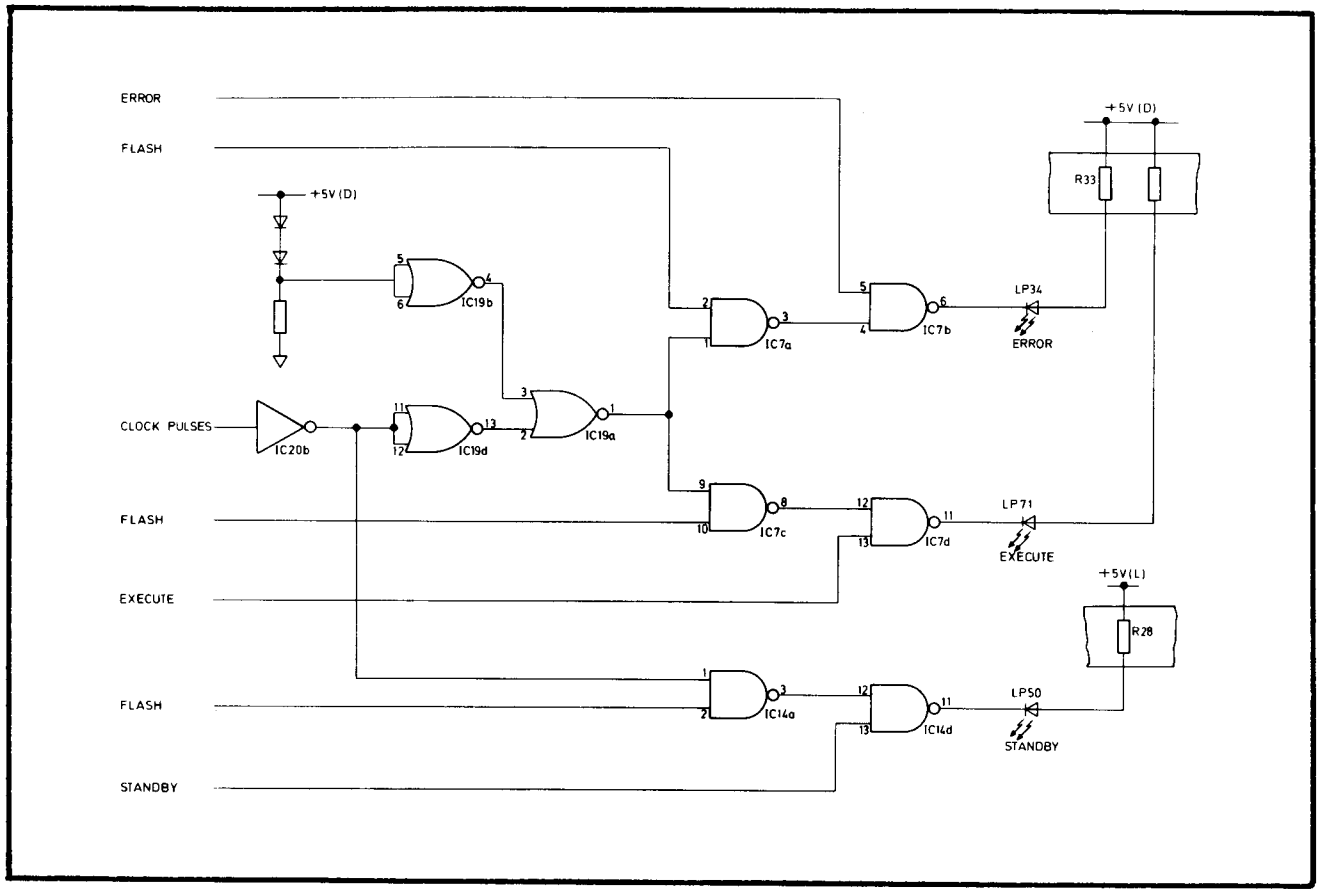


Fig. 6.10 Indicator Control Circuit

6.5.6.3.2 Each indicator has two control lines, an enable line, which is at logic '1' when an indication is required, and a flash line, which is at logic '1' when the indicator is required to flash.

6.5.6.3.3 The STANDBY indicator continues to function during periods of standby operation, since IC20 and IC14 are powered from the +5 V (L) rail. Since IC7 is powered from the +5 V (D) rail, the EXECUTE and ERROR indicators are inoperative in standby. To prevent random flashing of the indicators during power fade, the low voltage detector IC19b holds IC7/1 and 9 at logic '0'.

6.5.6.4 Display Check and Inhibit

6.5.6.4.1 For the display check, all the display elements are turned on, while for special function 30, all displays are blanked. This requires additional control circuitry for the external-modulation signal-level indicators and the BATTERY LOW indicator.

6.5.6.4.2 For the display check, the microprocessor sets data line D0 to logic '1' and addresses IC15 (CHKLED). This gives a logic '0' at IC15/11 and a logic '1' at IC15/10, which turns on the LEDs via IC14c, IC24 and IC25.

6.5.6.4.3 To inhibit the indicators, the microprocessor sets data line D1 to logic '1' and addresses IC15 (CHKLED). This gives a logic '0' at IC15/8, and the indicators are inhibited in IC14b, IC214, and IC25.

6.5.6.5 Spinwheel Pulse Generator

6.5.6.5.1 The optical coupling in Q1 and Q2 is by reflection from a disc attached to the spinwheel. This disc has alternate sections of high and low reflectance, so that pulses appear at TP2 and TP3 when the spinwheel is operated. The mechanical arrangement is such that there is a 90^{o} phase difference between the pulse waveforms. The pulses are shaped in IC5, and passed to the processor assembly via the motherboard assembly.

6.5.7 LF SYNTHESIZER, ATTENUATOR AND RPPU CONTROL

6.5.7.1 Introduction

6.5.7.1.1 The circuitry for deriving the voltage levels required on the control lines for the LF synthesizer, the output attenuator, the auxiliary input, and the reverse-power protection-unit (RPPU) is mounted on the motherboard assembly, 19-1043. The circuit diagram is given in Fig. 6 in Section 8 of this manual. The final level adjustment of the control signals for the LF synthesizer is made on the LF synthesizer assembly, 19-1047. The circuit is shown in Fig. 28 in Section 8.

6.5.7.2 Control Line Decoding

6.5.7.2.1 A number of local control lines are used on the motherboard. The logic levels on these lines are decoded from:

(a) the low-order address bits on lines A0 to A3

(b) the logic levels on the system control lines, decoded on the processor assembly from the high-order address bits.

6.5.7.2.2 The local control lines are shown in Table 6.8. Decoding takes place in IC7, selected by $\overline{\text{LATCH SELECT}}$, or IC22, selected by $\overline{\text{ATTEN SELECT}}$.

6.5.7.3 LF Control Line Setting

6.5.7.3.1 The control lines for the LF synthesizer carry analog signals, derived in the latched-input digital-to-analog converters IC14, IC4, IC11, IC5, IC12, IC6, and IC13. The output is referenced to the LF ground line (TP1). The reference voltage for the converters is taken across the band-gap diode, IC2.

6.5.7.3.2 To change the settings on the LF lines, the microprocessor addresses IC8 (LFBUFF) and puts a data byte on the bus. This data byte forms an address for the ROM, IC3 and IC9, which puts data onto the 16-line local bus. The microprocessor then addresses $\overline{\text{LFSEL}}$, and the ROM output is latched into IC14. The process is repeated to latch data into IC4 and IC11 ($\overline{\text{LFSEL+1}}$), IC5 and IC12 ($\overline{\text{LFSEL+2}}$), and IC6 and IC13 ($\overline{\text{LFSEL+3}}$).

6.5.7.3.3 The control lines pass to the LF synthesizer via the audio system assembly, 19-1048. On the LF synthesizer, two analog signals, designated VCO and VCF, are derived from each control line except LFO. Each of the VCF signal channels can be adjusted for level and gain (R5 and R30 for VCF6). The system reference voltage is derived from the band-gap diode IC2.

TABLE 6.8

Motherboard Assembly Local Control Lines

Decoder	Name	Use
IC7/12	$\overline{\text{AML}}$	Enables RF amplifier-bandwidth-control latch, IC27
IC7/11	$\overline{\text{LFSEL}}$	Select the latched digital-to-analog converters for the LF system control lines
IC7/10	$\overline{\text{LFSEL+1}}$	
IC7/9	$\overline{\text{LFSEL+2}}$	
IC7/7	$\overline{\text{LFSEL+3}}$	
IC22/1	$\overline{\text{ATTENA}}$	Enables the output-attenuator-control-line latch, IC16
IC22/2	$\overline{\text{LFBUFF}}$	Enables the LF system data latch, IC8
IC22/3	$\overline{\text{ATSTAT}}$	Enables the attenuator state buffer, IC21
IC22/4	$\overline{\text{PULSAT}}$	Triggers the attenuator pulsing monostable, IC20a
IC22/5	$\overline{\text{CLRIL1}}$	Clears the IL1 latch, IC25a
IC22/6	$\overline{\text{PROTLA}}$	Resets the RPPU relay and alarm
IC22/7	$\overline{\text{PROTUN}}$	Triggers the RPPU relay
IC22/8	$\overline{\text{TONEON}}$	Triggers the RPPU alarm for test
IC22/9	$\overline{\text{TONEOF}}$	Resets the RPPU alarm after test
IC22/10	$\overline{\text{CKTRIG}}$	Triggers the clunker monostable, IC19a
IC22/11	$\overline{\text{CLRAUX}}$	Clears the auxiliary interrupt latches, IC10 and IC17
IC22/13	$\overline{\text{RDAUX}}$	Enables the auxiliary input buffer, IC1

6.5.7.4 Output Attenuator Control Line Setting

6.5.7.4.1 The output attenuator is controlled by a series of five magnetically latched relays. Each relay has two coils, one to open the relay and one to close it. Because of the magnetic latching, voltage need only be applied to the coils when a change of state is required.

6.5.7.4.2 The procedure for resetting the attenuation is as follows:

(a) The microprocessor addresses $\overline{\text{ATSTAT}}$ and reads the states of IC20a and IC20b via IC21 and the data bus.

(b) When both circuits are in the reset state, $\overline{\text{ATTENA}}$ is addressed, and the data byte required to operate those attenuator relays which are to increase attenuation is entered into IC16. Because IC16/1 is held at logic '1' by IC20a, this information does not appear at the outputs.

(c) The microprocessor addresses $\overline{\text{PULSAT}}$. This triggers the monostable, IC20a, which enables the outputs of IC16 for approximately 40 ms. The interval is set by means of R21.

(d) Approximately 7.5 ms after addressing $\overline{\text{PULSAT}}$, the microprocessor again addresses $\overline{\text{ATTENA}}$, and puts the data byte required to operate those attenuator relays which are to reduce attenuation onto the bus. The outputs of IC16 are still enabled by IC20a, so the relays operate immediately.

(e) The trailing-edge of the pulse from IC20a triggers the monostable, IC20b. The pulse width is approximately 500 ms. This sets the maximum rate at which the attenuator setting can be updated, since no further change can be made until IC20b returns to the reset state.

6.5.7.5 RPPU Operation

6.5.7.5.1 If reverse power is applied at the instrument's RF output socket, the peak detectors in the RPPU will drive PL6 pin 1 positive. A logic '1' is then applied at IC23b/4. Provided the instrument is not at standby, IC23b/5 is also at logic '1', and a logic '0' is produced at IC23b/6. This sets IC25a, and triggers the monostable IC18b via IC23c. The pulse from IC18b drives the RPPU-relay-isolate coil through Q4/Q2, while the logic '0' at IC25a/6 forms the RPPU interrupt signal $\overline{\text{IL1}}$.

6.5.7.5.2 The RPPU interrupt also sets IC25b, via IC23a and IC24b, to put Q5 to the conducting state and sound the alarm.

6.5.7.5.3 When the cause of the interrupt has been established, the microprocessor switches the RF output off, and clears the RPPU interrupt by addressing $\overline{\text{CLRIL1}}$. When the RF output is switched on again, the microprocessor addresses $\overline{\text{PROTLA}}$, which triggers IC18a and clears IC25b. The pulse of IC18a drives the RPPU relay connect coil, while clearing IC25b mutes the alarm.

6.5.7.5.4 A ±14.3V power supply for the RPPU circuit is derived from the ±15V supply rails by Q13 and Q14. The base potentials of these transistors are controlled by the voltage at the junction of R3 and R6, fed back via Q15 and Q16, to maintain the RPPU supply balanced about 0V.

6.5.7.6 Output Amplifier Bandwidth Control

6.5.7.6.1 The logic level on the bandwidth control line at PL5 pin 14 is governed by control lines $\overline{\text{OPC2}}$, OPC3, and OPD11. These levels are set by the microprocessor addressing the appropriate latch and setting the necessary level on data line D3, D4, or D5. The control line is driven via Q17, Q11 and Q10. Transistors Q11 and Q10 provide a change of voltage level.

6.5.7.7 Clunker Drive

6.5.7.7.1 The clunker is driven by the monostable IC19a, Q6 and Q7. The monostable is triggered by the microprocessor addressing $\overline{\text{CKTRIG}}$. The monostable pulse length can be adjusted by means of R59.

6.5.7.8 Auxiliary Input Operation

6.5.7.8.1 If an auxiliary input at PL9 pin 6, 8, or 10 occurs, IC10a, IC17b, or IC17a will be clocked by the negative-going edge. An interrupt on IL15, IL16, or IL17 will result. Once the microprocessor has established the cause of the interrupt, it addresses $\overline{\text{RDAUX}}$ to enable IC1 and reads the data from the bus. It then addresses $\overline{\text{CLRAUX}}$ to clear the interrupt latches.

6.5.7.9 Alarm Test

6.5.7.9.1 To switch the alarm on and off for test purposes, the microprocessor addresses TONEON and TONEOF. These signals set and clear the alarm driver, IC25b.

6.5.7.9.2 The alarm may also be used as the touch panel annunciator in place of the clunker, by using special function 03. Control lines TONEON and TONEOF are used to operate the alarm for this purpose also.

6.5.8 THE GPIB INTERFACE

6.5.8.1 Introduction

6.5.8.1.1 The majority of the circuitry of the GPIB interface is carried on the GPIB assembly, 19-1050. This includes the ROM containing the GPIB program. The bus connector and the GPIB address setting switches are mounted on the GPIB connector assembly 19-1053. The circuit diagrams are given in Fig. 12 and Fig. 16. in Section 8 of this manual.

6.5.8.2 Address Setting and Recognition

6.5.8.2.1 When the interface address is set on the GPIB by the controller, it is recognized by the General Purpose Interface Adaptor (GPIA), IC5, by comparison with the interface address set in one of its internal registers. The interface address set on the rear-panel switches is read by the microprocessor and written into the GPIA address register on switching-on, during initialization, or when special function 40 is used.

6.5.8.2.2 The microprocessor sees the address switches as an addressable location within the GPIA. When the GPIA receives this address it responds by generating an enable signal, ASE, at IC5/4. This enables IC1, putting the inverse of the logic levels set by the switches onto the data bus. The microprocessor reads the data from the bus and then writes it into the GPIA address register.

6.5.8.3 Operation as a Listener

6.5.8.3.1 When the interface is addressed to listen the GPIA conducts the handshake routine up to the point where the ready for data (RFD) indication is given. At this point IC5/27 is at logic '0', setting the data line buffers in IC2 and IC3 to the receive condition. The data byte from the bus enters the GPIA data-in register, and when the data valid (DAV) message is sent true, an interrupt request is generated by IC5/40 going to logic '0'. This puts IC7/8 to logic '1' and pulls the IRQ line to logic '0' via IC4b.

6.5.8.3.2 The microprocessor interrupt routine which follows will establish the reason for the interrupt. The GPIA data-in register and IC18 are addressed, using the GPIB SELECT signal, decoded on the processor assembly from the high-order address bits, and address lines A0 to A3. The direction of data flow in IC18 is set by the R/W signal so that the data byte in the data-in register can be read by the microprocessor.

6.5.8.3.3 When the data transfer is complete, the GPIA cancels the interrupt request and allows the data accepted line (DAC) to go high. The handshake routine then continues, and a further data byte, if available, is loaded into the data-in register. The interrupt and data transfer routine is then repeated.

6.5.8.4 Operation as a Talker

6.5.8.4.1 When the GPIA is addressed to talk, the data-out register will normally be empty. Under these conditions an interrupt request is generated by IC5/40 going to logic '0', pulling the microprocessor $\overline{IRQ}$ line to logic '0' via IC7 and IC4b. The same signal also sets IC15a.

6.5.8.4.2 When IC15a is set, a logic '1' is applied to IC14/10. Since IC15b is normally reset, and IC5/27 is at logic '1' when the GPIA is addressed to talk, IC14/8 goes to logic '0'. The RFD line is open-circuited between TP1 and TP2, and IC5/18 is connected to 0 V by IC12. Even if the listening device asserts that it is ready for data, the GPIA will not attempt to load the contents of its data-out register onto the bus.

6.5.8.4.3 The microprocessor interrupt routine will establish the reason for the interrupt. The GPIA data-out register is addressed, and a data byte is written into the register.

6.5.8.4.4 Following the data transfer, the microprocessor sets data bus line DO to logic '0' and addresses the decoder, IC13, to direct the GPIBCLK signal to IC15a/11. This clocks IC15a to the reset condition, giving a logic '0' at IC14/10. The bilateral switches in IC12 reconnect the RFD line to the GPIA, and release IC5/18 from 0 V. When the listening device asserts ready-for-data, the GPIA loads the contents of the data-out register onto the bus and continues with the handshake sequence.

6.5.8.4.5 If, for any reason, the GPIA is taken out of the talk state partway through a message, the data-out register will be left containing an untransmitted byte. When the GPIA is readdressed to talk either of two requirements may apply. The GPIA may be required to continue with the interrupted message or may be required to transmit a byte other than the one held in the data-out register (e.g. the status byte, if a serial poll is to be conducted).

6.5.8.4.6 The two situations are distinguished by the state of IC15a. If the original message is to continue, IC10a will be in the reset condition, having been reset by the microprocessor after the data-out register was loaded. The RFD line will be connected to IC5/18 via IC12, and when the GPIA is addressed to talk the byte held in the data-out register will be transmitted.

6.5.8.4.7 If a serial poll is to be conducted, the GPIA is taken out of the talk state, addressed to listen, and receives the serial poll enable (SPE) message byte. In generating the interrupt required to transfer this message to the microprocessor, the GPIA sets IC15a, breaking the RFD line to IC5/18. As part of its serial poll routine the microprocessor addresses IC13 to direct the GPIBCLK signal to clock IC15b to the set state and IC15a to the reset state.

6.5.8.4.8 When the GPIA is addressed to talk, it is unable to complete the handshake procedure to transmit the byte in the data-out register because of the break in the RFD line. It is now necessary to generate a microprocessor interrupt so that the status byte will be written into the data-out register, overwriting the byte already there. This cannot be done by the GPIA since the data-out register is not empty, but when the listening device asserts ready-for-data, IC7/1 goes to logic '1'. Since the GPIA is addressed to talk IC7/13 is at logic '1', as is IC7/2, so the required microprocessor interrupt is generated by IC7/12 going to logic '0'.

6.5.8.4.9 Once the microprocessor has written the status byte into the GPIA data-out register, it sets data bus line D1 to logic '0' and addresses IC13 to direct the GPIBCLK signal to IC15b/3. This clocks IC15b to the reset state, giving a logic '1' at IC14/9, so reconnecting the RFD line to IC5/18 via IC12. The GPIA completes the handshake procedure and transmits the status byte.

6.5.8.5 Detection of the Serial Poll Disable Message

6.5.8.5.1 At the end of the serial poll sequence, the controller sends the serial poll disable (SPD) message. It is possible for IC15b to be in the set state when this occurs because not every device on the bus necessarily transmits its status byte. If this is the case the SPD message is detected in IC6 and resets IC15b.

6.5.8.6 Untalk, Unlisten and IFC Interrupt

6.5.8.6.1 Microprocessor interrupts are generated if the unlisten, untalk, or IFC message is received. The untalk and unlisten messages are multiline, and are decoded in IC11 to give a logic '0' at IC11/8, which sets IC10a. The IFC message is single line, and is applied to IC10a/3 to clock IC10 to the set state.

6.5.8.6.2 With IC10 set, IC7/9 is at logic '0' and the required interrupt is generated via IC4b. The interrupt is cleared by the microprocessor addressing IC13 to direct the GPIBCLK signal to IC10/1.

6.5.8.7 ATN Interrupt

6.5.8.7.1 An interrupt will be generated via IC9c and IC4b whenever the attention message (ATN) is sent false (ATN line high) provided IC9c is enabled. Enablement and disablement of IC9c are controlled by the microprocessor setting or resetting IC10b via IC13.

6.5.9 THE AUDIO SYSTEM ASSEMBLY

6.5.9.1 The operation of the control channel of the audio system assembly is described in paragraph 6.5.2.4.

6.5.10 THE FM SYSTEM ASSEMBLY

6.5.10.1 The circuit of the FM system decoder and control line latch is shown in Fig. 26 in Section 8 of this manual.

6.5.10.2 Four control lines are used for the FM system. The logic levels are held in the latch, IC3. When any change to the levels is required the microprocessor addresses IC3, using address lines A0 to A3 and the LATCH SELECT signal decoded on the processor board, and puts the required control line levels on data lines D0 to D3. The address is decoded in IC2 to provide a logic '0' at IC3/6 which enters the fresh data into the latch.

6.5.11 THE OUTPUT SYSTEM ASSEMBLY

6.5.11.1 The circuit of the output system decoder and control line latches is shown in Fig. 22 in Section 8 of this manual.

6.5.11.2 Five data latches, IC1 to IC5, hold the logic levels for nineteen control lines. When a change to the levels is required, the microprocessor addresses the appropriate latch, using address lines A0 to A3 and the LATCH SELECT signal decoded on the processor board, and puts the required control line levels on the data bus. The address is decoded in IC6 to give the correct latch enablement signal.

6.5.12 THE COMB LOOP ASSEMBLY

6.5.12.1 Introduction

6.5.12.1.1 The comb loop assembly is controlled via 20 binary and three analog control lines. The circuit for setting the levels on these lines is shown in Fig. 24 in Section 8 of this manual.

6.5.12.2 Decoder and Data Latches

6.5.12.2.1 The system uses five data latches, IC12, IC17, IC10, IC14, and IC16. The latch outputs are used for three purposes:

(a) For direct control of the logic level on a control line.

(b) To select a preset voltage level for an analog control line.

(c) To address a ROM, the output of which is used to determine a control line signal level.

6.5.12.2.2 When a change in the latch output is required, the microprocessor addresses the appropriate latch, using address lines A0 to A3 and the LATCH SELECT signal decoded on the processor board, and puts the required data on the data bus. The address is decoded in IC18 to give the correct latch enablement signal.

6.5.12.3 Directly Controlled Lines

6.5.12.3.1 The binary control lines OCAØ and OCA2 to OCA6 are set to levels held in latches IC14 and IC17. The level-on control line OCA1 is derived, via the NOR gate formed by IC4a and IC4f, from one output of each of IC12 and IC17.

6.5.12.4 Control Line OCB2

6.5.12.4.1 Control line OCB2 carries a preset analog voltage selected by means of the multiplexer, IC3. The multiplexer address is made up from three outputs from the latch, IC12, and one output from the ROM, IC9. The preset levels are adjusted during calibration by the variable resistors in R26, R27, and R28. The voltage applied to the potentiometers is supplied via the stabilizer containing Q1 and IC1a.

6.5.12.5 Control Lines OCBØ and OCB1

6.5.12.5.1 Outputs from the latches IC10, IC14, and IC16 are used to address the ROMs, IC7, IC9, IC13, and IC15. The ROM outputs provide the inputs to the digital-to-analog converters IC6 and IC11. The converter outputs are buffered and amplified in IC8 to provide the analog voltage levels for control lines OCBØ and OCB1.

6.5.12.6 ROM Controlled Lines

6.5.12.6.1 The logic levels on control lines OCA8 to OCA10 and OCDØ to OCD5 are taken direct from the outputs of ROMs IC9 and IC15.

6.5.13 THE POWER SUPPLY SYSTEM

6.5.13.1 Introduction

6.5.13.1.1 The power supply system components are mounted on the following assemblies:

(a) Chassis assembly, 11-1520
(b) Rear panel assembly, 11-1530
(c) Power unit chassis assembly, 11-1537
(d) Power supply interconnect assembly, 19-1058
(e) Power supply control assembly, 19-1059.

6.5.13.1.2 A circuit of the complete power supply system is given in Fig. 20 in Section 8 of this manual. There are ten supply rails, giving the supplies listed in Table 6.9. Seven of the rails are controlled by similar discrete-component systems, while three use integrated circuit regulators. A detailed description is given for one of each type of circuit only.

TABLE 6.9

Power Supply Rail Details

Voltage	Available at	Standby State
+24 V	SK12 pin 2	Switched off
+24 V (OVEN)	SK12 pin 4	Maintained
+18 V	SK12 pin 6	Maintained
+15 V	SK13 pin 12	Switched off
+5 V (A)	SK12 pin 1	Switched off
+5 V (D)	SK12 pin 5	Switched off
+5 V (G)	SK13 pin 3	Maintained
+5 V (L)	SK13 pin 7	Maintained
-5.2 V	SK13 pin 10	Switched off
-15 V	SK13 pin 11	Switched off

6.5.13.2 The +5 V (A) Supply

6.5.13.2.1 The +5 V (A) supply is typical of the supplies having discrete component regulators. The circuit diagram is given in Fig. 6.11.

6.5.13.2.2 The low-voltage AC supply from the power transformer is rectified by D6 and D7 to provide unregulated DC at pin 9 of the power-supply-interconnect assembly, 19-1058. This voltage is applied to the series regulator, Q7, via the +5 V (A) fuse, FS8. The regulated output from Q7 is taken via the current-sensing resistor, R13.

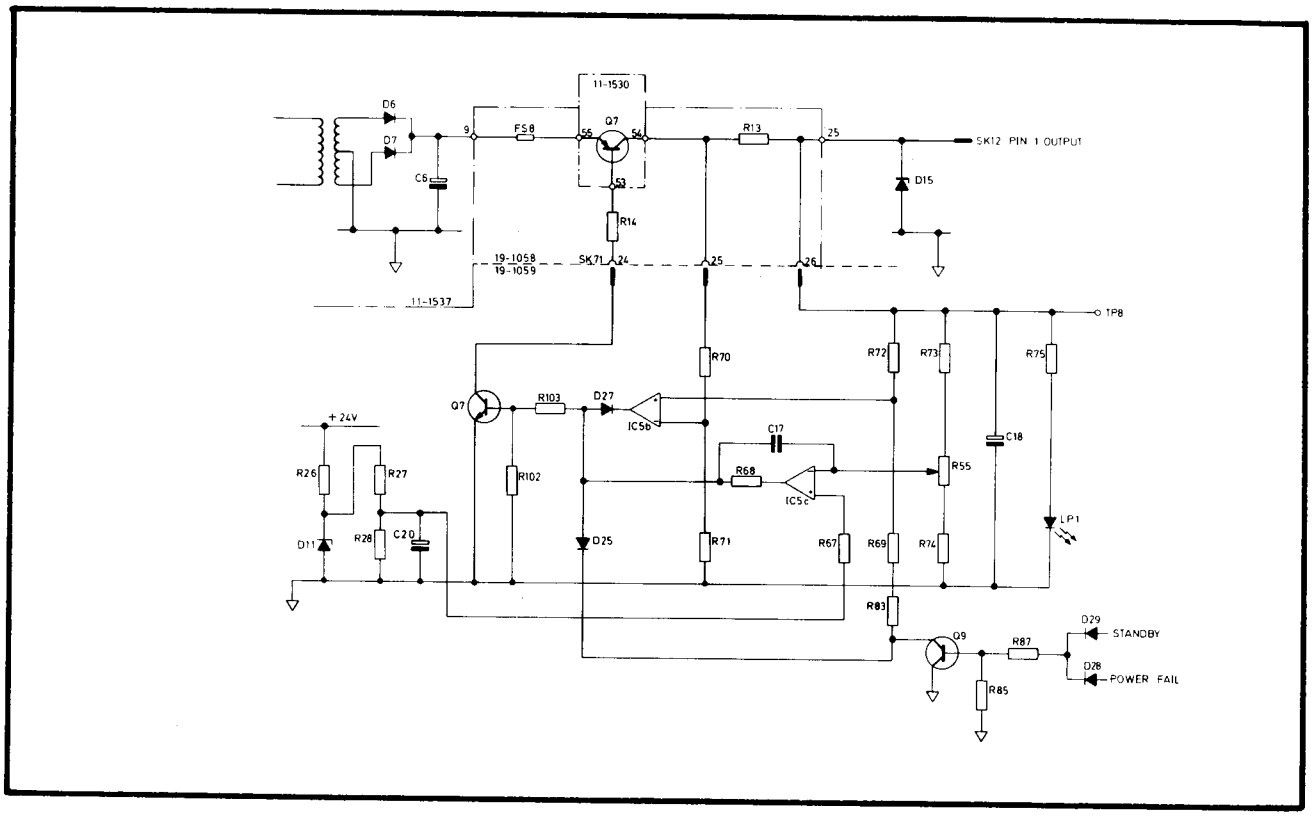


Fig. 6.11 The +5 V (A) Power Supply

6.5.13.2.3 The regulated voltage appears across the resistor chain R73, R55, R74. A proportion of this voltage, at the wiper of R55, is compared with a reference voltage, developed across R28, in IC5c. The output of IC5c controls the current in Q7, and sets the base current of the series regulator so as to maintain the required output voltage. Adjustment of the output voltage is made by means of R55.

6.5.13.2.4 The volt drop in R13 is proportional to the current drawn from the supply. If the voltage at the R72/R69 junction goes negative with respect to that at the R70/R71 junction, the output of IC5b goes low. The base of Q7 is pulled low via D27, reducing the base current of the series regulator and the output current.

6.5.13.2.5 When the microprocessor puts the standby control line to logic '1', Q9 conducts. The base of Q7 is pulled low via D25 to shut down the supply. Note that no diode equivalent to D25 is fitted to the +5 V (L) supply, which maintains power in the standby condition. The -5.2 V and -15 V supplies are shut down by Q8, which is cut off when Q9 conducts.

6.5.13.2.6 The indicator LP1, located adjacent to the fuse FS8, lights when the supply is on, and provides a quick check of whether the supply is functioning.

6.5.13.3 The +18 V Supply

6.5.13.3.1 The +18 V supply is typical of the supplies having integrated circuit regulators. The circuit diagram is given in Fig. 6.12.

6.5.13.3.2 The supply has a conventional, negative-line stabilizer circuit. The diode D1 is incorporated to protect the stabilizer from reverse current. This can arise due to the discharge of electrolytic capacitors in the supplied circuit when the equipment is switched off.

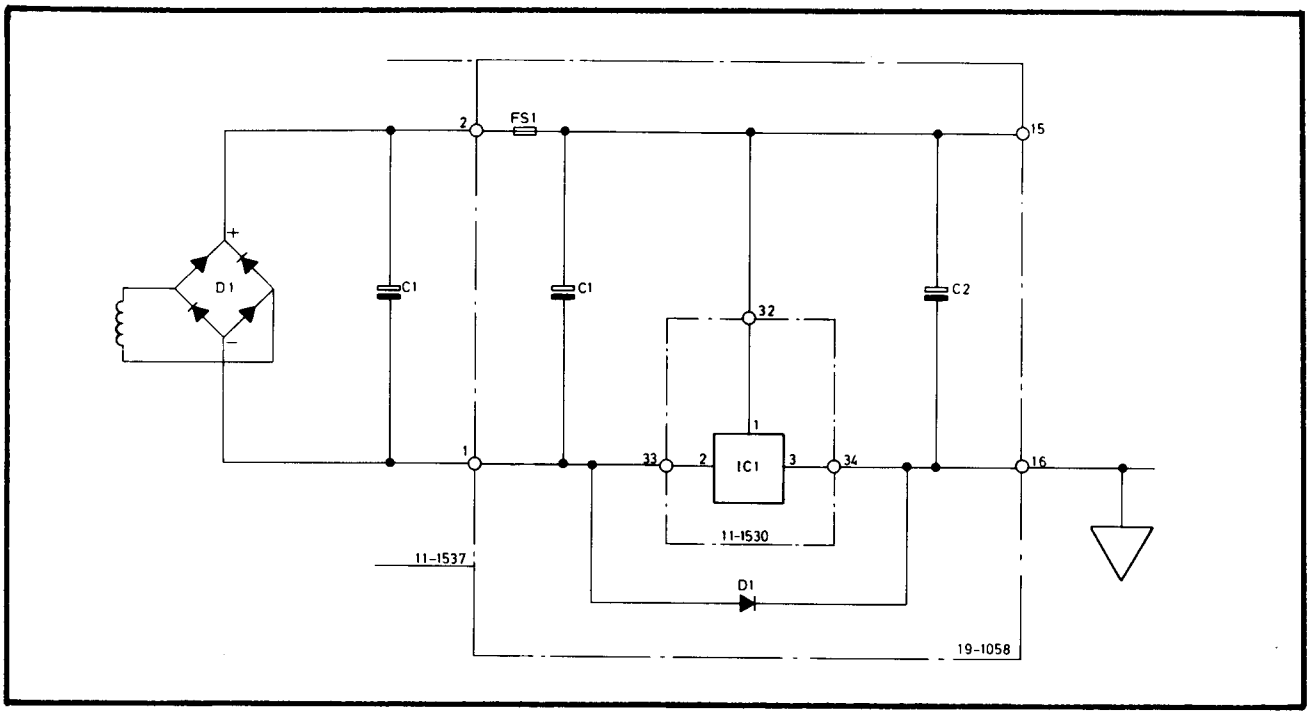


Fig. 6.12 The +18 V Power Supply

6.5.13.4 The Overtemperature Interrupt

6.5.13.4.1 The temperature-sensing circuit is shown in Fig. 6.13. The comparator, IC5d, compares the voltage from the R27/R28 junction with that from the TH1/R23 junction. The thermistor is mounted close to the series regulators. If the voltage at IC5d/12 falls below that at IC5d/13 the logic '0' at IC5d/14 forms the $\overline{\text{OVTEMP}}$ interrupt to the microprocessor.

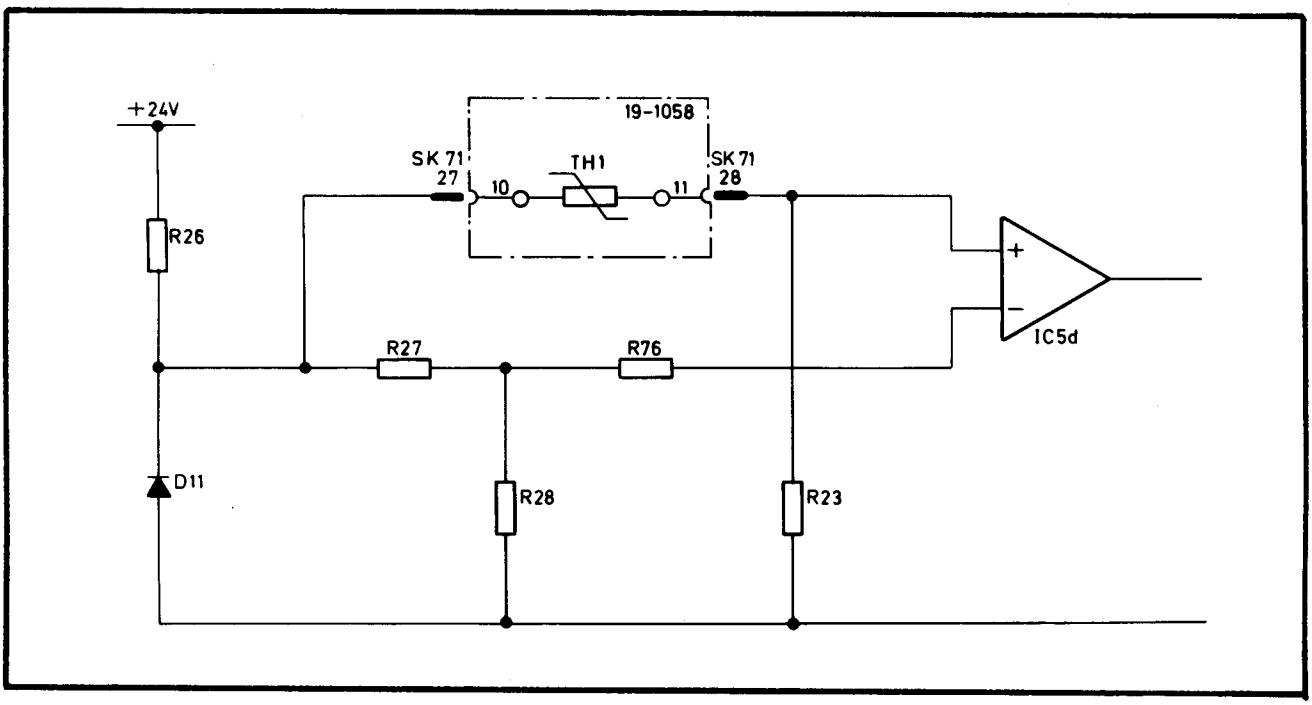


Fig. 6.13 Temperature-Sensing Circuit

6.5.13.5 $\overline{\text{PWRDN}}$ Interrupt

6.5.13.5.1 When the AC supply is connected to the power transformer, C19 on assembly 19-1059 is charged from D8 and D9 on assembly 11-1537. The voltage across C19 will be greater than that applied at IC5a/2, IC5a/1 will be at logic '1' and Q10 will conduct. If the supply is switched off or fails, C19 will discharge through R78 and IC5a/3 will become more negative than IC5a/2. The output of IC5a will go to logic '0', providing the $\overline{\text{PWRDN}}$ interrupt to the microprocessor, and Q10 will be cut off. The positive-going transition at the collector will be fed to Q9 via D28, putting the power supplies to the standby condition. This ensures that the power supply rails hold up for as long as possible, to give the microprocessor time to store the instrument's status.

SECTION 7 MAINTENANCE

7.1 INTRODUCTION

7.1.1 This section is in seven parts, providing information on:

(a) Details of automatic indications of fault conditions.

(b) Details of special functions for fault diagnosis.

(c) Signature analysis information.

(d) Fault finding on the RF system.

(e) Setup procedures to be carried out on owner-repairable assemblies following repair.

(f) Dismantling and reassembly instructions.

(g) Overall specification check.

7.2 TEST EQUIPMENT REQUIRED

7.2.1 A complete list of the test equipment required to carry out the procedures described in this section is given in Table 7.1 The items required for each operation are listed at the start of the relevant paragraph.

7.2.2 Although the procedures to be followed are given in general terms they are based on the use of the recommended item of test equipment. Some modification to the procedures given may be necessary if equipment other than the recommended model is used. The parameters given in Table 7.1 are those necessary to permit the required measurements to be made.

7.3 AUTOMATIC INDICATIONS OF FAULT CONDITIONS

7.3.1 INTRODUCTION

7.3.1.1 A number of points in the circuit are monitored, either continuously or on specified occasions, during operating. An automatic indication is given if a fault condition arises. Such indications are additional to any error codes which may be generated by the same fault.

7.3.1.2 The forms of indication given are shown in Table 7.2. A more detailed explanation is given in the following paragraphs.

TABLE 7.1

Test Equipment Required

Item	Description Recommended Model	Required Parameters
1	Signature analyzer HP 5004	
2	Frequency counter Racal-Dana 9919	To measure 1.1 GHz with 1 Hz resolution
3	Measuring Receiver HP 8902A and HP 11722A	100 dB dynamic range with 0.1 dB resolution
4	Wattmeter HP 436A and HP 8482A	To measure from 3 dBm to 21 dBm with 0.1 dB resolution over the frequency range from 1 MHz to 1.3 GHz
5	Audio Analyzer HP 8903A	To measure signal level and distortion at frequencies of 400 Hz and 1 kHz
6	Audio Signal Generator Racal-Dana 9083	Frequency 1 kHz with output level from 0 V to 2.2 V r.m.s. into 600 Ω.
7	Spectrum Analyzer HP 8566A	Minimum sweep width of 3.9 GHz.
8	DC Supply	Output variable from 0 V to 2.5 V into 16 kΩ
9	Spectrum Analyzer System HP 3047A	To measure noise levels below -150 dBc/Hz
10	Oscilloscope HP 1740A	Bandwidth 10 MHz Dual trace
11	Frequency Standard Racal-Dana 9475	1 MHz

TABLE 7.1 (Continued)

Test Equipment Required

Item	Description Recommended Model	Required Parameters
12	Signal Generator Racal-Dana 9087	Frequency 9.999900 MHz to 10.000100 MHz accurate to ±1 Hz. Residual FM less than 1 Hz
13	Frequency Distribution System Racal-Dana 9478	To give 1 MHz and 10 MHz output from 1 MHz and 10 MHz input
14	Spectrum Analyzer HP 8568 A	
15	Calibrated Attenuator Pads	10 dB, 20 dB, 40 dB and 80 dB
16	True RMS Voltmeter Racal-Dana 5002	To measure over the range 0 V to 3 V r.m.s. at frequencies up to 10 MHz
17	Distortion Analyzer HP 334A	To measure THD to an accuracy of 0.1% up to 3% at frequencies from 400 Hz to 100 kHz
18	Modulation Analyzer HP 8901A	To measure FM of carrier frequencies up to 1 GHz
19	Coaxial notch filter	125 mm length of RG 58 cable, with one Type N connector and one open circuit end.
20	T piece	Type N connectors
21	Service Support Kit Racal-Dana 11-1579	Contains extender boards and wrenches for coaxial connectors

TABLE 7.2

Fault Indications

Indications	Associated Error Code	When Test is Made	Fault
Instrument inoperative with displays blank.	01	At switch-on	Processor RAM fault.
Instrument inoperative with two-digit number in frequency display	02	At switch-on. On initial-ization. Special function 00	Program ROM checksum error
Instrument inoperative with two-digit number in frequency display	03	At switch-on	Stuck key
Two-digit number in frequency display. (Error indication clears when instrument is operated)	51	At switch-on. Special function 71	Non-volatile memory fault
One digit in frequency display alternates between normal and -	80 to 88	Continuous	Out-of-lock error
One digit in frequency display alternates between normal and ⊟	90 to 97	Continuous	Power supply failure.

7.3.2 THE PROCESSOR RAM CHECK

7.3.2.1 The processor assembly RAM, IC13 on assembly 19-1051, is checked for function. If a fault is found, error code 01 is generated and the check is repeated. This continues, with the instrument inoperative, until the fault is cleared.

7.3.2.2 The check involves writing to and reading from the RAM, and therefore checks the operation of the RAM selection and enabling circuits as well as the operation of IC13.

7.3.3 THE PROGRAM ROM CHECK

7.3.3.1 A checksum test is carried out on each ROM position in turn. The order of checking is shown in Table 7.3. If a fault is found the number of the ROM position will be shown in the frequency display. The faults which can be detected are:

(a) ROM IC not present.
(b) ROM IC contents corrupted.
(c) ROM IC fitted in wrong position.
(d) Version number of ROM IC fitted does not match that of IC12.

TABLE 7.3

Order of ROM Check

Check order	ROM Position Number	Circuit Identification
1	9	IC 12
2	8	IC 11
3	7	IC 10
4	6	IC 9
5	5	IC 8
6	4	IC 7
7	3	IC 6
8	2	IC 5
9	1	IC 4
10	10	IC 17 (19-1050)

7.3.4 STUCK KEY CHECK

7.3.4.1 If a fault is found, error code 03 is generated and the key code number appears in the frequency display. The key codes are shown in Table 7.4.

7.3.5 NON-VOLATILE MEMORY CHECK

7.3.5.1 Each RAM on assembly 19-1049 is checked in turn. The check involves reading and writing to each IC. It therefore checks the operation of the IC selection signal decoding circuits and the clock signal circuits as well as the RAM ICs. The RAM contents are not changed by the check.

7.3.5.2 If a fault is found, error code 51 is generated and the IC number of the RAM concerned appears in the frequency display. The display will be cleared if the instrument is operated using either the front-panel controls or the GPIB. However, data recall from the non-volatile memory may be impossible.

7.3.6 OUT-OF-LOCK ERRORS

7.3.6.1 Provided that the generation of out-of-lock errors is not inhibited by the use of special function 08, loss of lock in a phase-locked loop will result in the generation of an error code and the flashing of a digit in the frequency display. The digit which flashes and the error code generated depend on which loop has lost lock, as shown in Table 7.5.

7.3.6.2 The AGC loop of the output system is also monitored. If a fault occurs, the least significant digit of the amplitude display flashes. The corresponding error code is 88.

TABLE 7.4

Key Codes

Code	Key	Code	Key
01	Special Funct	42	7
02	8	43	4
03	5	44	1
04	2	45	0
05		46	Backspace
06	Store		
07	Memory Exch	50	FM
		51	M
11	Display Error Code	52	FM/Phase On/Off
12	9	53	FM/Phase Int 400
13	6	54	FM/Phase Int 1000
14	3	55	FM/Phase Ext AC
15	-	56	FM Ext DC
16	Recall		
17	Exec	60	AM
		61	Pulse
22	Hold	62	AM/Pulse On/Off
23	Fine	63	AM/Pulse Int 400
24	Medium	64	AM/Pulse Int 1000
25	Coarse	65	AM/Pulse Ext DC
26	Step	66	AM/Pulse Ext AC
27	Step up		
		70	Local
		71	Frequency
32	GHz/V	72	Step size
33	MHz/mV	73	Relative
34	kHz/µV	74	Amplitude
35	Hz/mV	75	Init
36	%/Rads/dB	76	Standby
37	Step Down	77	Output On/Off

TABLE 7.5

Out-of-Lock Indications

Fault Location	Flashing Digit	Error Code
Reference generator	10^7 Hz	80
Output loop	10^6 Hz	81
Comb loop	10^5 Hz	82
FM phase-locked loop	10^4 Hz	83
FM frequency-locked loop	10^3 Hz	84

TABLE 7.6

Power Supply Failure Indications

Fault Location	Flashing Digit	Error Code
+24 V oven supply	10^7 Hz	97
+18 V	10^6 Hz	96
+24 V	10^5 Hz	95
+15 V	10^4 Hz	94
+5 V (A)	10^3 Hz	93
+5 V (D)	10^2 Hz	92
-5.2 V	10 Hz	91
-15 V	1 Hz	90

7.3.7 POWER SUPPLY FAILURES

7.3.7.1 The power supply rails, with the exception of the +5 V (L) rail, are individually monitored. Failure of a rail will result in the generation of an error code and the flashing of a digit in the frequency display. The digit which flashes and the error code generated depend on which supply rail has failed, as shown in Table 7.6.

7.3.7.2 The +5 V (D) supply powers the display, so the fault indication may not be seen. The error code is still generated, and may be read via the GPIB.

7.4 SPECIAL FUNCTIONS FOR FAULT DIAGNOSIS

7.4.1 INTRODUCTION

7.4.1.1 A number of special functions are provided as an aid to fault diagnosis. These are additional to the special functions for operator use given in Section 4 page 4-50, but are enabled and disabled in the same manner.

7.4.1.2 Brief details of the additional special functions are given in Table 7.7. A more detailed explanation is given in the following paragraphs.

TABLE 7.7

Special Functions for Fault Diagnosis

Special Function Number	Function
00	Checks contents and position of each program ROM.
11	Selects frequency as the primary function and clears frequency relative, if set. Displays the LF synthesizer output frequency.
12	Selects frequency as the primary function and clears frequency relative, if set. Displays the comb loop frequency
13	Selects frequency as the primary function and clears frequency relative, if set. Displays the output loop frequency.
24	Displays contents of interrupt buffer for IL2 to IL9 (IC31 on assembly 19-1051).
25	Displays contents of interrupt buffer for IL10 to IL17 (IC32 on assembly 19-1051).
26	Displays contents of interrupt buffer for IL18 to IL25 (IC42 on assembly 19-1051).
27	Displays number held in spinwheel counter (IC14 and IC28 on assembly 19-1051).
30	Blanks all display elements.
32	Exercises display elements, all on - all off.
33	Exercises display elements, each element on and off in sequence.
34	Exercises all system latches.
35	Exercises outputs of decoder IC22 on assembly 19-1043.
36	Sweep outputs of LF system digital-to-analog converters (IC4, IC5, IC6, IC11, IC12, IC13 and IC14 on assembly 19-1043).
37	Sweep outputs of comb loop assembly.
52	Pulses and times the reverse-power protection-unit relay monostables (IC18a and IC18b on assembly 19-1043).
75	Exercises the valid-power latch, IC5a on 19-1049.
90	Pulses and times attenuator and clunker monostables (IC20a, IC20b, and IC19a on assembly 19-1043).
91	Sets amplitude system digital-to-analog converter input to 0800 (hexadecimal) and selects 0 dB output attenuation.
92	Sets amplitude system digital-to-analog converter input to 0870 (hexadecimal) and selects 0 dB output attenuation.
98	Enters non-maskable interrupt routine. Displays contents of interrupt buffer for IL1, OVTEMP, AUXIRQ1, AUXIRQ2, SWIRQ, KBDIRQ, GPIBIRQ and PWRDN.

7.4.2 SPECIAL FUNCTIONS 11, 12, AND 13

7.4.2.1 Special functions 11, 12, and 13 permit the frequencies which should exist at certain selected points in the RF generating system to be displayed. The measured frequency at these points can be compared with the displayed figure to check the functioning of the sealed modules.

7.4.2.2 The points at which the displayed frequency should be found are shown in Table 7.8. Note that the frequencies other than those at 11-1534 SK49 and 11-1535 SK60 will be frequency-modulated by any signals applied at 11-1535 SK65.

TABLE 7.8

RF System Measurement Points

Special Function	Displayed Frequency Measurement Points
11	11-1534 SK49 11-1535 SK60 and SK59 11-1702 SK38
12	Not measurable outside module 11-1702
13	11-1702 SK37 11-1532 SK32 and SK28 Only with RF output 11-1526 SK66 and SK1 greater than 650 MHz RF output socket selected.

7.4.2.3 The output frequency, and therefore the displayed frequency, can be changed by means of the spinwheel or the numerical keyboard while special function 11, 12, or 13 is in use. When the keyboard is used, the output frequency is displayed, in MHz, while the units key of the entry is held pressed. When the key is released the frequency display will revert to showing the relevant loop frequency.

7.4.3 SPECIAL FUNCTIONS 24, 25 and 26

7.4.3.1 Special functions 24, 25 and 26 display the contents of the buffers for interrupt lines IL2 to IL25 in the frequency display. The appearance of the display is as shown in Fig 7.1. Note that the occurrence of an interrupt is represented by a '1' in the display, regardless of the active level of the related interrupt line. The servicing of interrupts is inhibited while these special functions are active, so that the buffers will not be cleared while the contents are being examined.

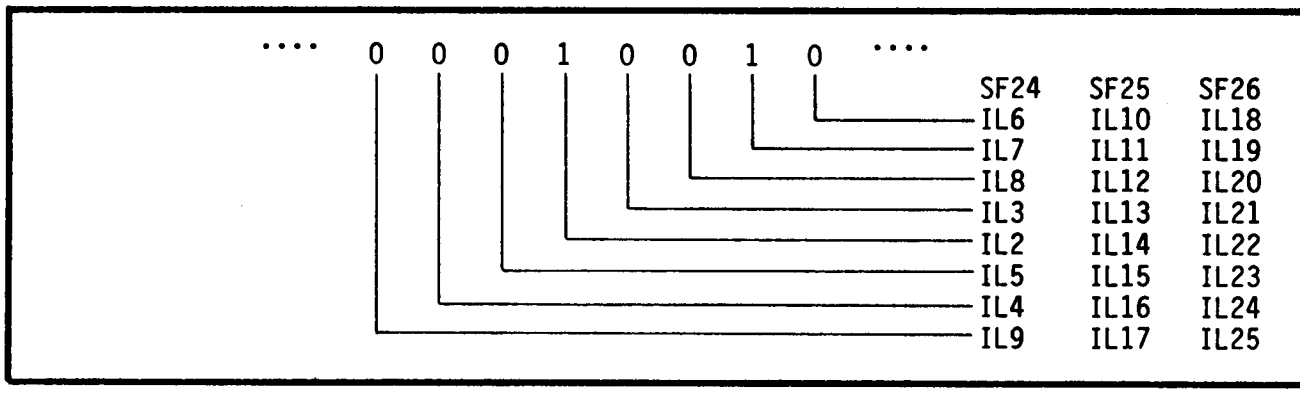


Fig 7.1 Interrupt Buffer Display

7.4.4 SPECIAL FUNCTION 27

7.4.4.1 Special function 27 permits the number held in the spinwheel counter to be displayed in decimal format. The limits of the number displayed are -128 and +127. The servicing of the spinwheel interrupt is inhibited while the special function is active, so the number in the counter can be varied to check the operation of the spinwheel circuitry.

7.4.5 SPECIAL FUNCTIONS 30, 32 AND 33

7.4.5.1 Special functions 30, 32 and 33 provide a complete check of the display function, as follows:

(a) Special function 30 checks that all display elements can be controlled to the "off" state. Note that special function 31, given in the list of special functions for operator use in Section 4 page 4-52, is available to check that all elements are functioning. Since the display is static during the checks, detailed examination of, for example, the individual elements of a numeric display is possible.

(b) Special function 32 switches the displays between all "on" and all "off". All the displays should appear to light, but with a lower than normal intensity. The numerical displays show the test pattern. If any display element has an intensity markedly above or below that of the others the operation of the relevant latch should be checked.

(c) Special function 33 switches on each display element in the following order:

(1) The numerical displays are switched "on" and "off", in sequence, five times, showing 1, 2, 4, 8 and .0.

(2) The legends and indicators except HIGH, LOW, BATT. LOW, STANDBY, ERROR, and EXEC are switched on and off in turn.

(3) The HIGH, LOW and BATT. LOW indicators light for approximately five seconds.

(4) The STANDBY, ERROR, and EXEC indicators flash for approximately five seconds.

If a numerical indicator fails to show the correct digit, the functioning of the indicator and the associated latch address decoder should be checked. If two displays light at the same time, check for display-line short circuits.

7.4.5.2 Care should be taken not to leave the instrument with special function 30 enabled, as in this condition it appears to be inoperative.

7.4.6 SPECIAL FUNCTION 34

7.4.6.1 With special function 34 enabled the outputs of all the system latches are first set to logic '1', then to logic '0'. For all latches directly connected to the data bus, the output should be a squarewave with a period of approximately 730 µs. The latch enable waveform will be pulses of approximately 0.4 µs every 370 µs.

7.4.7 SPECIAL FUNCTION 35

7.4.7.1 Special function 35 exercises the outputs at pins 3 ($\overline{\text{ATSTAT}}$), 5 ($\overline{\text{CLRIL1}}$), 8 ($\overline{\text{TONEON}}$), 9 ($\overline{\text{TONEOF}}$), 11 ($\overline{\text{CLRAUX}}$), 13 ($\overline{\text{RDAUX}}$), 15 (TP15), 16 (TP16) and 17 (TP17) of IC22 on assembly 19-1043. The output at each pin will be pulses of approximately 0.5 µs every 150 µs.

7.4.8 SPECIAL FUNCTION 36

7.4.8.1 Special function 36 provides a test waveform, in the form of a rising staircase at the output of each of the digital-to-analog converters on assembly 19-1043. The steps are not all the same height, but the outputs of all the converters should be identical. The waveform, which can be observed at test points 2 to 8, relative to the analog ground at TP1, is shown in Fig 7.2.

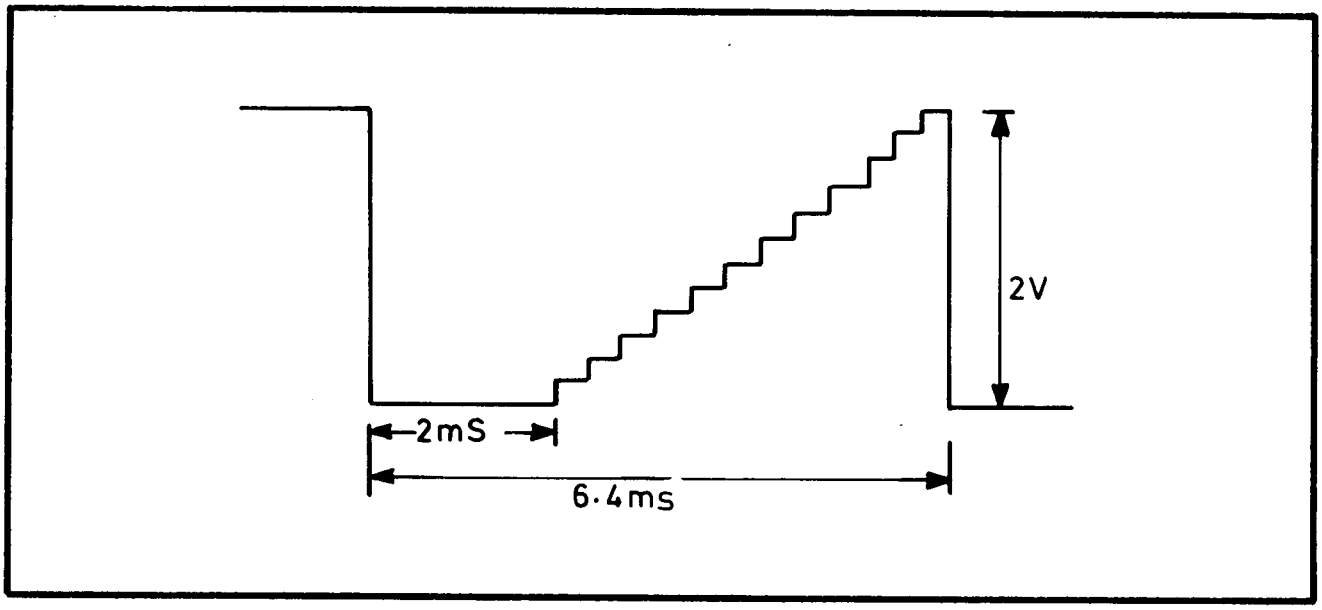


Fig 7.2 D-to-A Converter Sweep Waveform

7.4.9 SPECIAL FUNCTION 37

7.4.9.1 Special function 37 provides test waveforms at the outputs of the digital-to-analog converters on assembly 19-1045. The waveforms, which can be observed at links LK1 and LK2 are shown in Fig 7.3.

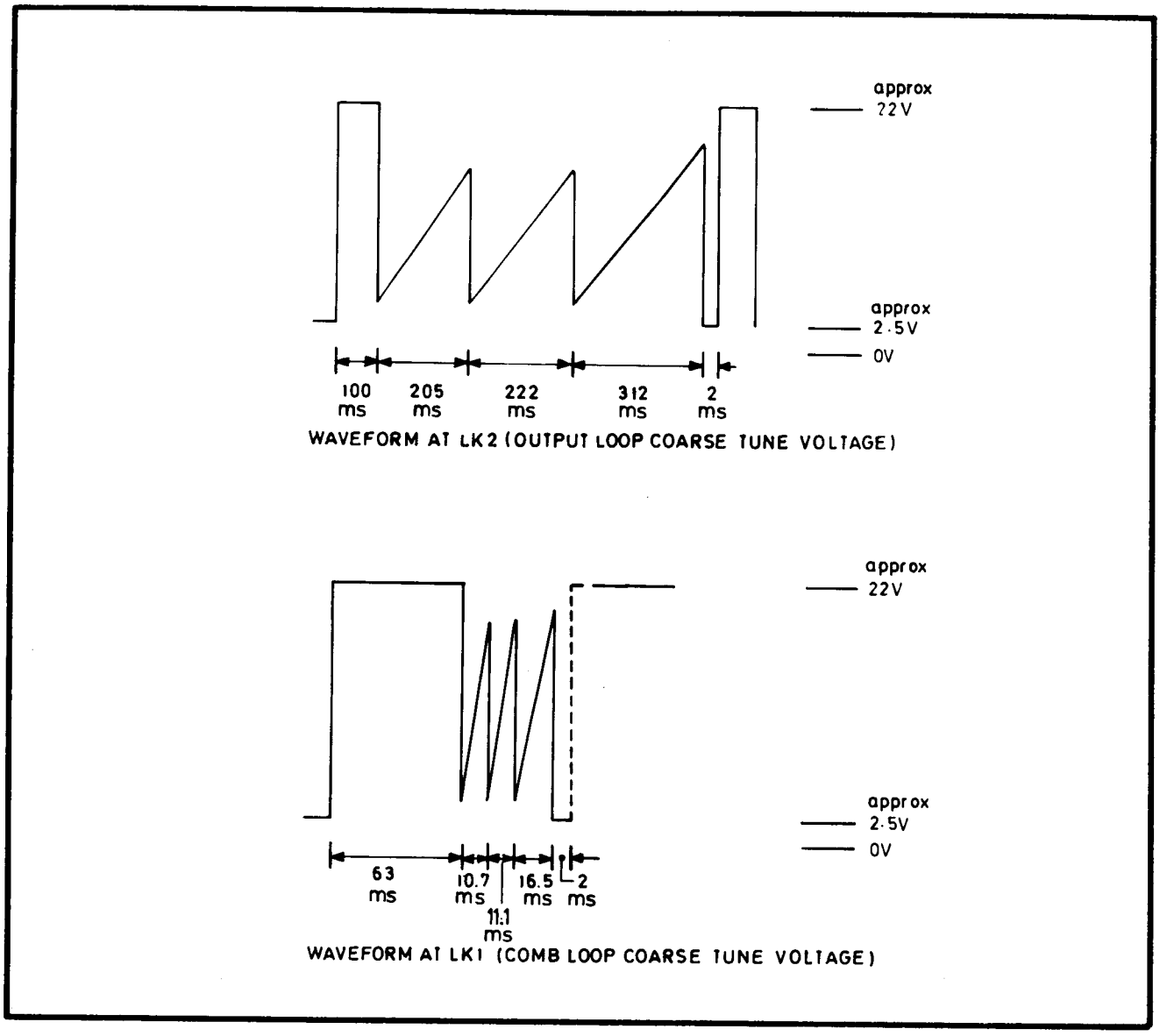


Fig 7.3 D-to-A Converter Test Waveforms

7.4.10 SPECIAL FUNCTION 52

7.4.10.1 Special function 52 permits the operation and timing of the reverse-power protection-unit relay-drive monostables to be checked. The durations of the monostable pulses are measured and displayed, in milliseconds, in the frequency display, as shown in Fig 7.4. Both pulse durations should be between 30 ms and 55 ms. The timing sequence is repeated, and the display updated, twice per second.

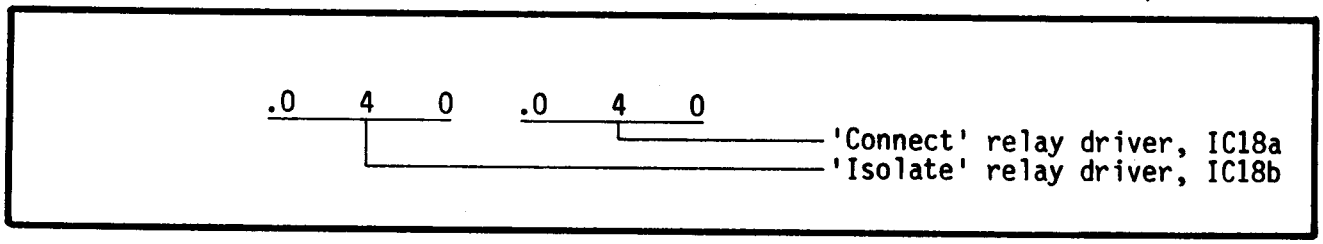


Fig 7.4 Monostable Timing Display

7.4.11 SPECIAL FUNCTION 75

7.4.11.1 Special function 75 checks the operation of the valid-power latch, IC5a, on assembly 19-1049. The latch is switched between the set and clear states approximately every 90 µs, and a corresponding squarewave should be observed at TP1.

7.4.12 SPECIAL FUNCTION 90

7.4.12.1 Special function 90 permits the operation and timing of the output attenuator and clunker drive monostables to be checked. The duration of the monostable pulses are measured and displayed, in milliseconds, in the frequency display, as shown in Fig 7.5. The timing sequence is repeated and the display updated twice per second.

7.4.12.2 The clunker time is set by R59 on assembly 19-1043, and should be 5.0 ms. The attenuator pulse time is set by R21 on assembly 19-1043, and should be 40 ms. The attenuator delay time is nonadjustable, but should be between 380 ms and 660 ms.

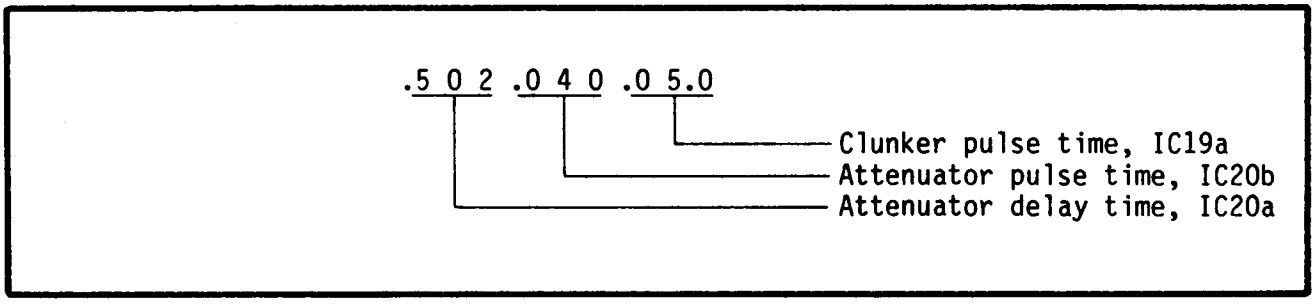


Fig 7.5 Monostable Timing Display

7.4.12.3 While special function 90 is enabled, the sections of the output attenuator are switched in and out of circuit, in turn, by the attenuator drive monostable to exercise the relays.

7.4.13 SPECIAL FUNCTIONS 91 AND 92

7.4.13.1 Special functions 91 and 92 set special values in the digital-to-analog converters of the output system during output system calibration.

7.4.14 SPECIAL FUNCTION 98

7.4.14.1 Special function 98 puts the microprocessor into its non-maskable interrupt routine. The contents of the first interrupt buffer are displayed in the frequency display, as shown in Fig 7.6. The occurrence of an interrupt is represented by a '1' in the display. The servicing of interrupts is inhibited while the special function is active, so that the buffer will not be cleared while the contents are being examined. If a key is pressed, the key code appears in the modulation display and the beeper sounds.

7.4.14.2 To leave special function 98, the instrument must be switched off.

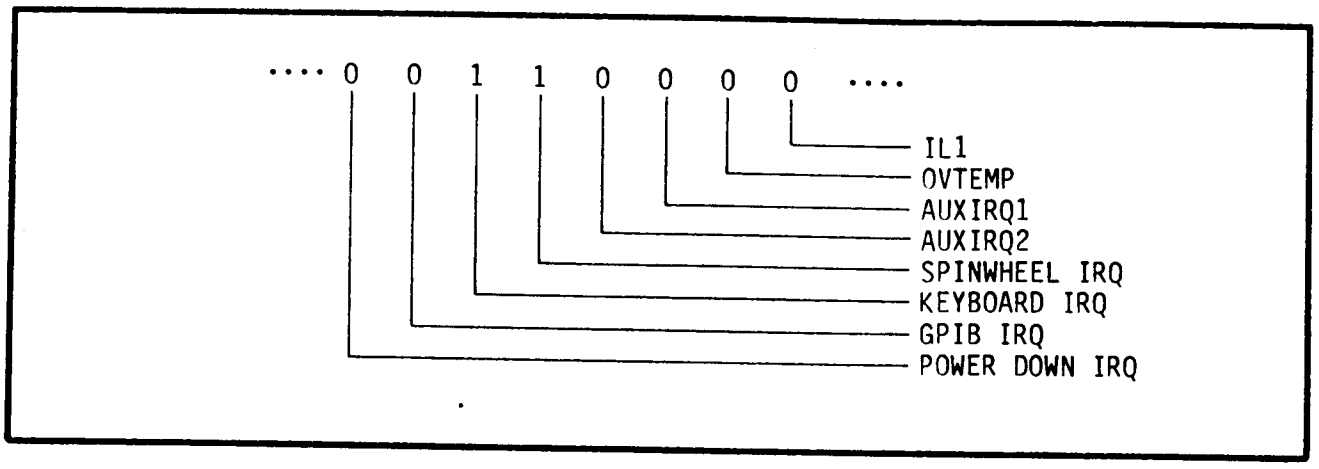


Fig 7.6 Interrupt Buffer Display

7.5 SIGNATURE ANALYSIS

7.5.1 TEST EQUIPMENT

7.5.1.1 The test equipment required is:

Item	Table 7.1 Item No
Signature Analyzer	1

7.5.2 PREPARATION FOR SIGNATURE ANALYSIS

7.5.2.1 Switch off the instrument and disconnect the AC supply. Remove the top cover, as instructed in paragraph 7.8.2. If signature analysis is to be performed on the motherboard, 19-1043, or the display assembly, 19-1041, remove the module block as instructed in paragraph 7.8.4. If analysis is to be performed on the module block, tilt the block within the chassis as instructed in paragraph 7.8.4.1 (a) to (g). If analysis is to be performed on the GPIB assembly, 19-1050, the assembly should be mounted on an extender board after the signature analyzer is connected. Disconnect the drive to the clunker from assembly 19-1041 to prevent overheating.

7.5.2.2 Mount the processor assembly, 19-1051, on an extender board. Set the IBE, LBE, IRQ, NMI, and HALT switches on the assembly to the open position, where the slider is towards the bottom of the board. Set the SIGNATURE ANALYSIS switch to the closed position, where the slider is towards the top of the board.

7.5.3 CONNECTING THE SIGNATURE ANALYZER

7.5.3.1 Connect the signature analyzer to assembly 19-1051 as follows:

(a) CLOCK input to TP9, negative-edge trigger

(b) START and STOP to TP12, negative-edge trigger

(c) GROUND to TP3

7.5.3.2 Set the HOLD and SELF TEST switches on the analyzer to OFF.

7.5.4 ANALYSIS PROCEDURE

WARNING: THIS PROCEDURE REQUIRES THE INSTRUMENT TO BE OPERATED WITH THE COVERS REMOVED. LETHAL VOLTAGE LEVELS ARE EXPOSED UNDER THESE CONDITIONS.

7.5.4.1 Connect the 9087 to the AC supply and switch the instrument on. Apply the probe of the analyzer to the points given in Tables 7.9 to 7.15 and check that the correct signatures are obtained.

TABLE 7.9

Signature Analysis, Assembly 19-1051

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC17 Pin 1	P13P	IC21 Pin 1	PF44	IC23 Pin 24	0003
2	784F	2	PF47	IC24 Pin 1,2	0003
3	1P10	3	C11H	3	7074
4	4787	4	C11P	4	PF63
5	11P2	5	0000	5	54F7
6	F47C	6	0003	6	A713
7	C11H	7	0000	7	AA68
8	PF44	8	0002	8	0000
9	UC12	9	0001	9	CH26
10	7PF7	10	0000	10	A3UU
11	SUC2	11	0003	11	H75C
12	0000	12	CH25	12	CA13
13	17PU	13	CH26	13	6039
14	45UB	14	0003	14	546H
15	917H	IC23 Pin 1	3838	15	826H
16	645F	2	7633	16	0003
17	H914	3	160H	IC25 Pin 1	0000
18	0000	4	04UU	2	P763
19	PF63	5	CFHU	3	6F9A
20	P763	6	57HU	4	8484
21	8484	7	96FA	5	U759
22	FFFF	8	546H	6	FFFF
23	UUUU	9	CA13	7	0356
24	0003	10	H75C	8	UUUU
IC18 Pin 1	645F	11	A3UU	9	1U5P
2-3	0000	12	0000	10	0000
4	917H	13	AA68	11	1U5P
5	917P	14	A713	12	UUUU
6	917H	15	54F7	13	0356
7	0000	16	6039	14	FFFF
8	0003	17	826H	15	U759
9	0000	18	0000	16	8484
10	0003	19	0002	17	6F9A
11	0000	20	9UP1	18	P763
12	0003	21	4868	19	0000
13	F47C	22	4FCA	20	0003
14	0003	23	6U28		

TABLE 7.9 (Continued)

Signature Analysis, Assembly 19-1051

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC26 Pin 1	0000	IC35 Pin 1	0000	10	47UA
2-6	0003	2	6U28	11	0003
7	0000	3	0001	12	0000
8	0003	4	37C5	13,14	0003
9	UUUU	5	9UP1	IC45 Pin 1	7074
10	FFFF	6	6321	2	PF63
11	8484	7	4868	3	2F1U
12	P763	8	7791	4	09UA
13	1U5P	9	4FCA	5	79CA
14	0356	10	0000	6	AUCC
15	U759	11	4FCA	7	2H91
16	6F9A	12	7791	8	A8HP
17	7791	13	4868	9	7423
18	6321	14	6321	10	APC2
19	37C5	15	9UP1	11	47UA
20	6U28	16	37C5	12	0000
21	0000	17	0001	13	54H4
22	4FCA	18	6U28	14	4P23
23	4868	19	0000	15	A98A
24	9UP1	20	0003	16	F077
25	0001	IC36 Pin 1,2	0003	17	04HU
26	0000	3	0000	18	0000
27	0003	4	7423	19	0001
28	0000	5	APC2	20	9UP1
29-35	0003	6	HA91	21	4868
36-38	0000	7	0000	22	4FCA
39,40	0003	8	132P	23	6U28
		9	54H4	24	0003

TABLE 7.10

Signature Analysis, Module 11-1535

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC2 Pin 1	UUUU	IC2 Pin 7	2861	IC2 Pin 13	896F
2	FFFF	8	0000	14	25CP
3	8484	9	A18A	15	96U4
4	0000	10	8626	16	0003
5	2H91	11	1895		
6	P763	12	6258		

TABLE 7.11

Signature Analysis, Assembly 19-1043

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC1 Pin 1	H1AU	IC11 Pin 4	CHH8	14	C468
2	0003	8,9	0000	15	AH19
3	3026	10	0003	16	2C45
4	H1AU	IC12 Pin 4	6U75	17	FAH2
5	0003	8,9	0000	18	A8HP
6	321C	10	0003	19	0000
7	0000	IC13 Pin 4	5CHP	20	P763
8	29F0	8,9	0000	21	8484
9	0003	10	0003	22	FFFF
10	H1AU	IC14 Pin 4	U76U	23	UUUU
11,12,13	0000	8,9	0000	24	0003
14	0003	10	0003	IC23 Pin 1	AF46
IC3 Pin 8	0000	IC16 Pin 10	0000	2	0003
15	917P	11	705H	3	AF45
16	0003	20	0003	4	0000
IC4 Pin 4	CHH8	IC17 Pin 4,7	0000	5	917H
8,9	0000	10	46C2	6	0003
10	0003	11	0000	7	0000
IC5 Pin 4	6U75	13	46C2	8	C117
8,9	0000	14	0003	9	C114
10	0003	IC18 Pin 1	F45U	10	0003
IC6 Pin 4	5CHP	2	0003	11	AU4H
8,9	0000	8,9	0000	12	F45U
10	0003	10	C117	13	6C12
IC7 Pin 1	UUUU	11,16	0003	14	0003
2	FFFF	IC19 Pin 1	1AF7	IC24 Pin 1	917P
3	8484	2,3	0003	2	917H
4	2H91	8-11	0000	3	AF45
5	P763	16	0003	4	AF46
6	0003	IC20 Pin 1	45F2	5	0000
7	5CHP	2,3	0003	6	0003
8	0000	8,9	0000	7,8	0000
9	6U75	11,16	0003	9	0003
10	CHH8	IC21 Pin 1	1706	10	AU4P
11	U76U	8,12	0000	11	AU4H
12	HHC0	15	1706	12	0003
13	76FH	16	0003	13	0000
14	HC38	IC22 Pin 1	705H	14	0003
15	6FPH	2	5F14	IC25 Pin 1	1173
16	0003	3	1706	2,3	0000
IC8 Pin 1	0000	4	45F2	4	0003
20	0003	5	1173	5	0000
IC9 Pin 8	0000	6	F45U	6	0003
15	917P	7	C114	7	0000
16	0003	8	AF46	8	AF46
IC10 Pin 1	0003	9	6C12	9	AF45
7	0000	10	1AF7	10	AF46
10	46C2	11	46C2	11,12	0000
11	0000	12	0000	13	AU4P
13	46C2	13	H1AU	14	0003
14	0003				

TABLE 7.12

Signature Analysis, Assembly 19-1041

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC3 Pin 1	0000	IC4 Pin 19	0000	IC16 Pin 13	1U5P
2,3	P763	20	P763	14	AUCC
4	0000	21	8484	15	0000
5,6	8484	22	FFFF	16	0003
7	0000	23	UUUU	IC17 Pin 1	8058
8,9	FFFF	24	0003	2	P015
10	0000	IC11 Pin 1	UUUU	3	3806
11,12	UUUU	2	FFFF	4	8P02
13	0000	3	8484	5	A383
14	0003	4	2370	6	28P3
IC4 Pin 1	65C5	5	P763	7	FA3C
2	596P	6	0003	8	728H
3	9658	7	142C	9	5FA0
4	6595	8	0000	10	572C
5	5966	9	50A3	11	15F9
6	965A	10	4282	12	0000
7	P595	11	0A07	13	8571
8	7966	12	2811	14	A15U
9	1P5A	13	A049	15	2854
10	F795	14	812C	16	4A16
11	C1P6	15	04A2	17	1286
12	0000	16	0003	18	AU34
13	6F7A	IC16 Pin 1,2	0000	19	0000
14	5C1H	3	0356	20	P763
15	16F4	8	0000	21	8484
16	05C2	9	818H	22	FFFF
17	016U	10	AU34	23	UUUU
18	H18H	11	2370	24	0003

TABLE 7.13

Signature Analysis, Assembly 19-1048

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC41 Pin 1	UUUU	IC41 Pin 14	49AC	IC49 Pin 7	2861
2	FFFF	15	26A2	8	0000
3	0003	16	0003	9	A18A
4,5	09UA	IC49 Pin 1	UUUU	10	8626
6,7	0003	2	FFFF	11	1895
8	0000	3	8484	12	6258
9-11	0003	4	0000	13	896F
12	C499	5	2H91	14	25CP
13	H269	6	P763	15	96U4
				16	0003

TABLE 7.14

Signature Analysis, Assembly 19-1050

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC1 Pin 1	5C20	IC9 Pin 9	0003	IC17 Pin 6	8484
10	0000	10	3A78	7	FFFF
19	5C20	14	0003	8	UUUU
20	0003	IC10 Pin 1	A7C6	9	11C7
IC5 Pin 1,2	0000	2-4	0003	10	2A9P
3	5878	5	0000	11	H737
4	5C20	6	0003	12	0000
5,6	0003	7	0000	13	CP20
19,20	0003	8	3A78	14	5AUH
27,28	0000	9	3A7C	15	HF3A
37	UUUU	10	3A78	16	HOP4
38	FFFF	11,12	0000	17	2231
39	8484	13	4P9H	18	57HU
40	0003	14	0003	19	37C5
IC7 Pin 1	0003	IC13 Pin 1	UUUU	20	0000
2	0000	2	FFFF	21	0003
3-5	0003	3	8484	22	6321
6-8	0000	4	P760	23	7791
9-12	0003	5	79CA	24	0003
13	0000	6	0003	IC18 Pin 1	0003
14	0003	7	13A4	10	0000
IC8 Pin 3	P763	8	0000	19	2P66
4	P760	9	4P9H	20	0003
5	79CA	10	3A78	IC16 Pin 7	0000
6	79C9	11	P99P	8	2P66
7	0000	12	A7C6	9	0003
14	0003	13	9PH6	10	2P65
IC9 Pin 1	9PH6	14	7C55	11	2P65
2	0003	15	PH58	12	57HU
3	2231	16	0003	13	79CA
4	P9PP	IC17 Pin 1	6F9A	14	0003
5	0000	2	U759		
6	5AUH	3	0356		
7	0000	4	1U5P		
8	3A7C	5	P763		

TABLE 7.15

Signature Analysis, Module 11-1532

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC6 Pin 1	UUUU	IC6 Pin 7	5CHP	IC6 Pin 13	76FH
2	FFFF	8	0000	14	HC38
3	8484	9	6U75	15	6FPH
4	2H91	10	CHH8	16	0003
5	P763	11	U76U		
6	0003	12	HHCO		

TABLE 7.16

Signature Analysis, Assembly 19-1049

LOCATION	SIGNATURE	LOCATION	SIGNATURE	LOCATION	SIGNATURE
IC19 Pin 1	0000	11	0000	IC15 Pin 13	132P
2	6321	12	0003	14	6U28
3	0356	IC18 Pin 13	0000	15	37C5
4	7791	14	0003	IC15 Pin 16	0003
5	1U5P	IC8 Pin 1	0003	IC22 Pin 1	0000
6	6F9A	2	0000	2,3	FFFF
7	P763	3	0000	4	0000
8	U759	4	0003	5,6	UUUU
9	8484	5	3242	7	0000
10	0000	6	3241	8,9	0003
11	8484	7	0000	10	0000
12	U759	8	0000	11,12	0003
13	P763	9	0003	13	0000
14	6F9A	10	2F1F	14	0003
15	1U5P	11	2F1U	IC12 Pin 1	2F1F
16	7791	12	F9CF	2	0003
17	0356	13	F9CU	3	2F1U
18	6321	14	0003	4	0003
19	0000	IC15 Pin 1	7H78	5	3241
20	0003	2	0958	6	3242
IC18 Pin 1	0000	3	2F18	7	0000
2	0000	4	82A9	8	0003
3	0000	5	U50U	9-11	0000
4	0000	6	C2U6	12-14	0003
5	F9CF	7	6696	IC20 Pin 1	0003
6	F9CU	8	0000	10	0000
7	0000	9	3241	19	F9CF
8	F9CF	10	9HHA	20	0003
9	HA91	11	F128		
10	132P	12	F9CF		

7.6 FAULT LOCATION

7.6.1 A guide to fault location is given in the flow charts of Fig. 7.7 to Fig. 7.12. The charts provide a logical procedure for locating a fault to module level. The module block should be removed from the 9087, and connected to the chassis using the connectors provided in the Service Support Kit, Racal-Dana part number 11-1579.

7.6.2 When using the charts it is essential to commence at Chart A and act according to the results of each decision box met in turn. Starting part way through any chart may lead to unsatisfactory fault location.

7.6.3 Unless otherwise specified in the charts all measurements should be made with the measured signal loaded with 50 Ω.

7.6.4 Where relevant, signature analysis should be carried out on any module which is indicated as being faulty before the module is exchanged.

7.7 SETTING UP AFTER REPAIR

7.7.1 INTRODUCTION

7.7.1.1 After repair of an assembly, the relevant tests given in the following paragraphs should be carried out before performing the overall specification test.

7.7.2 DISPLAY ASSEMBLY 19-1041

7.7.2.1 With the display assembly mounted in the 9087, check the operation of the display elements using special functions 30, 31, 32, and 33. Details are given in paragraphs 7.4.5.

7.7.2.2 Check the operation of the spinwheel counters using special function 27 (see paragraphs 7.4.4). Turn the spinwheel one complete turn counterclockwise and check that the displayed number increases continuously from 000 to 060 with no missed values. Turn the spinwheel one turn clockwise and check that the displayed number decreases to 000 with no missed values.

7.7.3 NON-VOLATILE MEMORY ASSEMBLY 19-1049

7.7.3.1 Test equipment required:

Item	Table 7.1 Item No.
True RMS Voltmeter	16
Frequency Counter	2
Oscilloscope	10
Extender Board 19-1121	21

7.7.3.2 Preparation for Testing

7.7.3.2.1 (a) Fit the extender board, but not assembly 19-1049, to the 9087. Ensure that the extender board switch is set to NORMAL.

(b) Connect the voltmeter to measure the direct voltage at TP1 on the extender board relative to 0 V on the 9087.

(c) Switch on the 9087. If necessary adjust the potentiometer on the extender card until the voltmeter indicates 2.2 V.

(d) Switch off the 9087. Disconnect the voltmeter.

(e) Insert assembly 19-1049 into the extender board.

7.7.3.3 VALID-POWER Signal Test

7.7.3.3.1 Connect the oscilloscope, using DC coupling, to monitor TP1 on assembly 19-1049. Switch on the 9087 and wait five seconds for the processor to complete the startup sequence.

7.7.3.3.2 Carry out the test as follows:

(a) Initialize the 9087.

(b) Activate special function 75. Check that the figure 75 appears in the AMPLITUDE display.

(c) Check that the oscilloscope displays a squarewave having a low level of less than 0.8 V and a high level of more than 2 V. The period of the waveform should be approximately 180 µs.

(d) Turn the spinwheel. Check that the oscilloscope display remains at the high level of the squarewave displayed in (c).

(e) Switch off the 9087 and disconnect the oscilloscope.

7.7.3.4 Battery Voltage Threshold Setting

7.7.3.4.1 Set the switch on the extender board to the SET position. Turn R17 on assembly 19-1049 fully clockwise.

7.7.3.4.2 Carry out the test as follows:

(a) Switch on the 9087. Check that the BATT LOW indicator is extinguished.

(b) Turn R17 slowly counterclockwise until the BATT LOW indicator lights.

(c) Switch off the 9087. Set the switch on the extender board to NORMAL.

(d) Switch on the 9087. Check that the BATT LOW indicator is extinguished.

7.7.3.5 Battery Charging Time Test

7.7.3.5.1 Carry out the test as follows:

(a) Activate special function 70.

(b) Check that the BATT LOW indicator is lit.

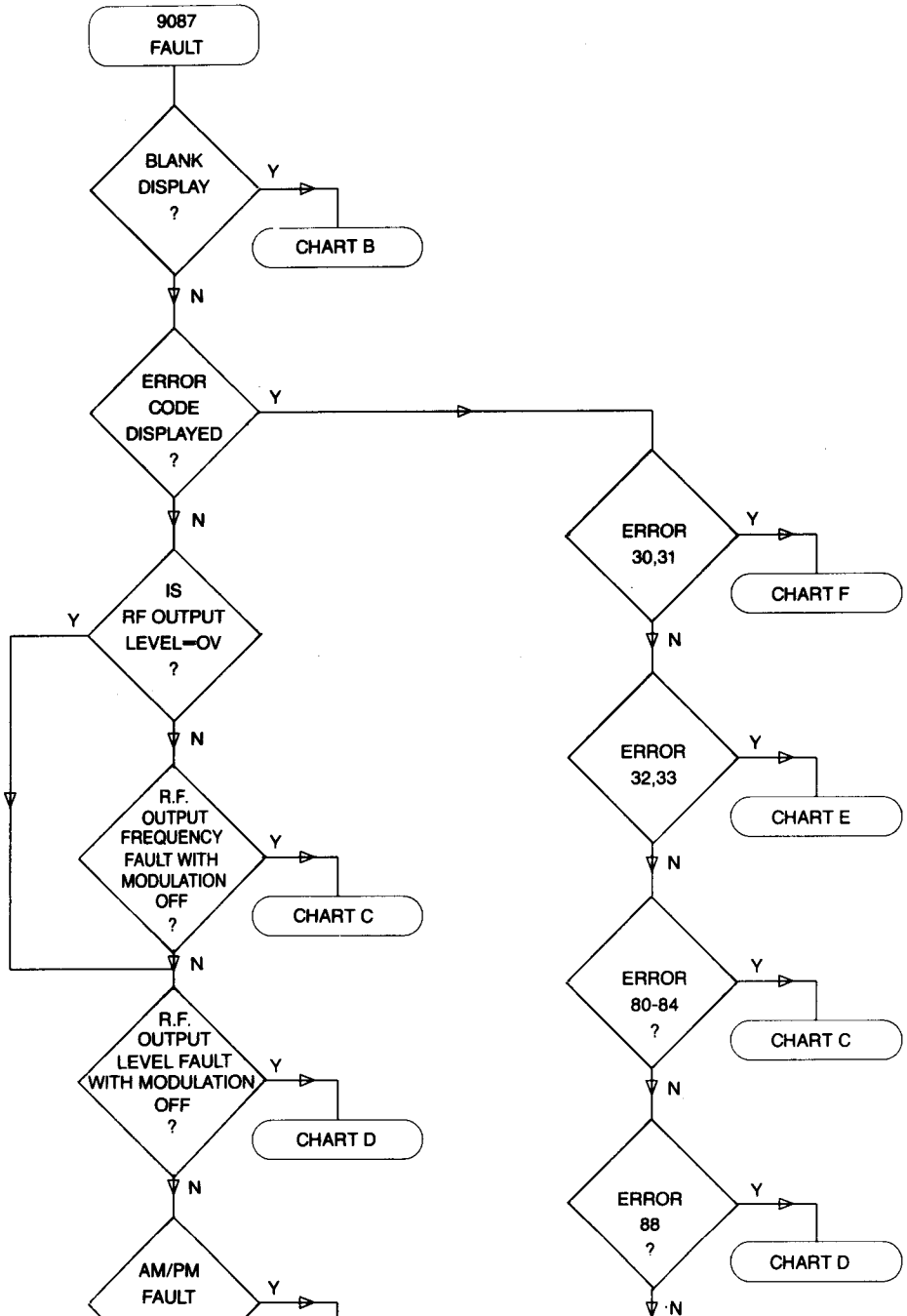
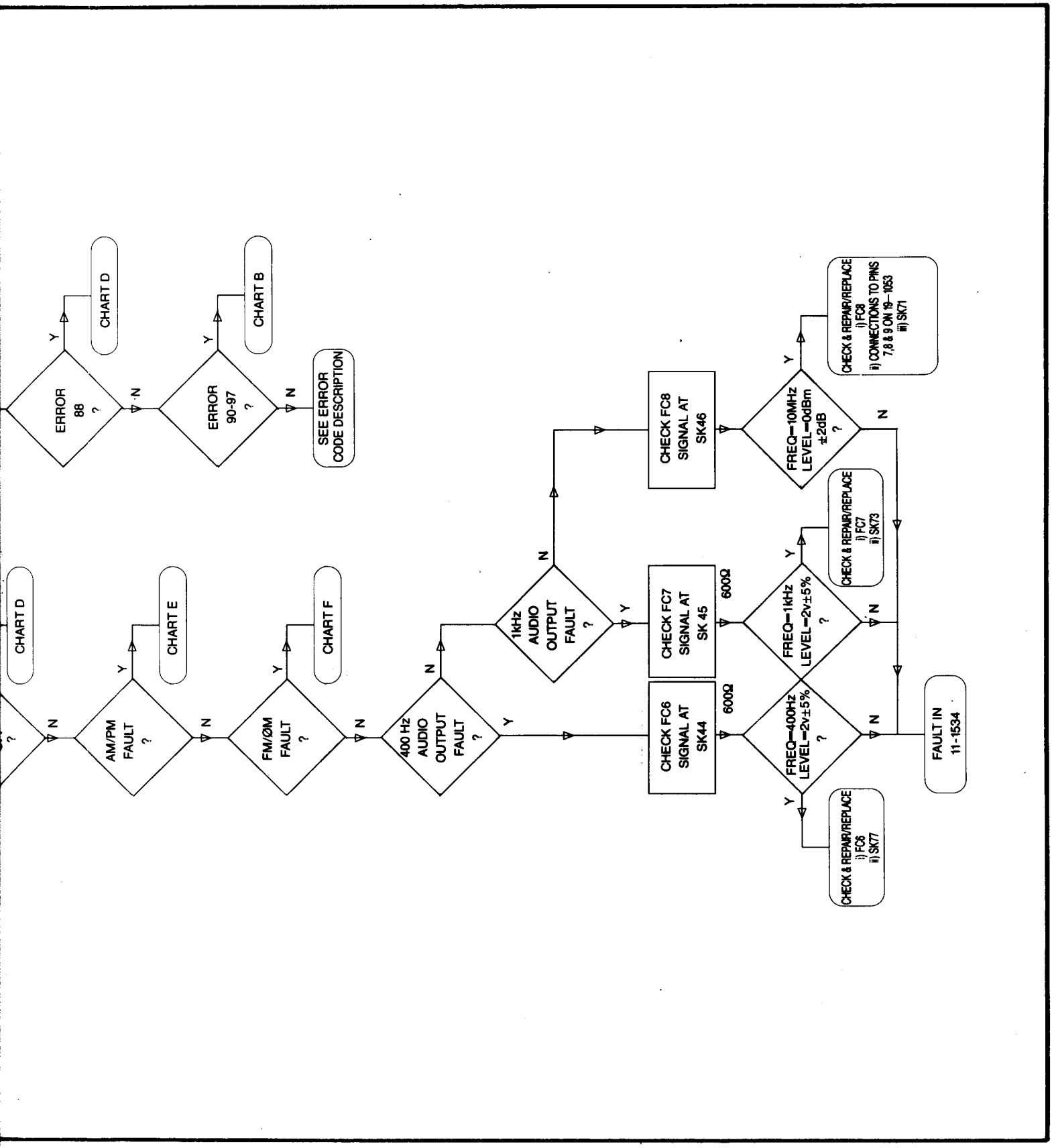


Fig. 7.7 Fault Finding P



ault Finding Procedure - Chart A

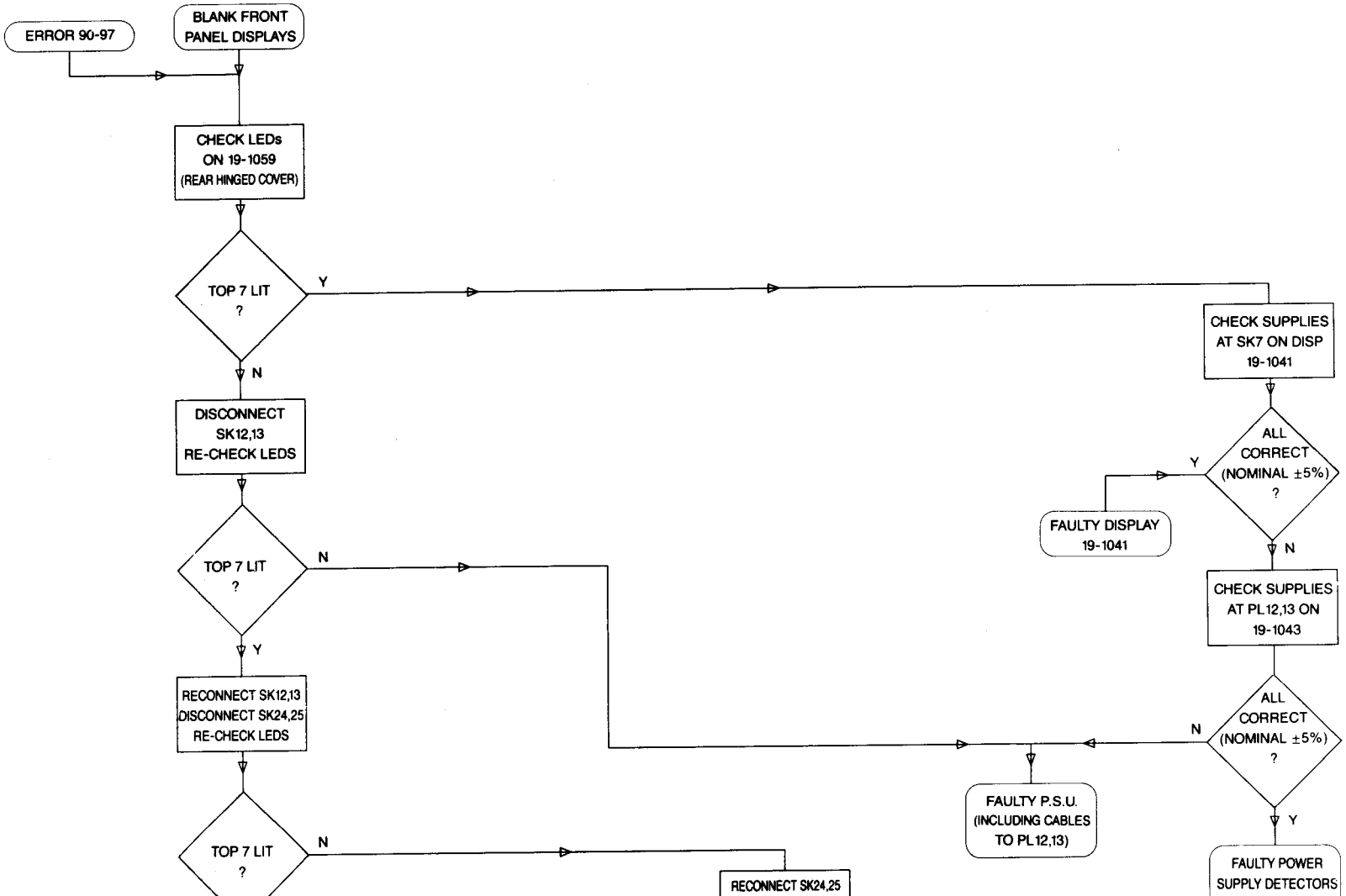
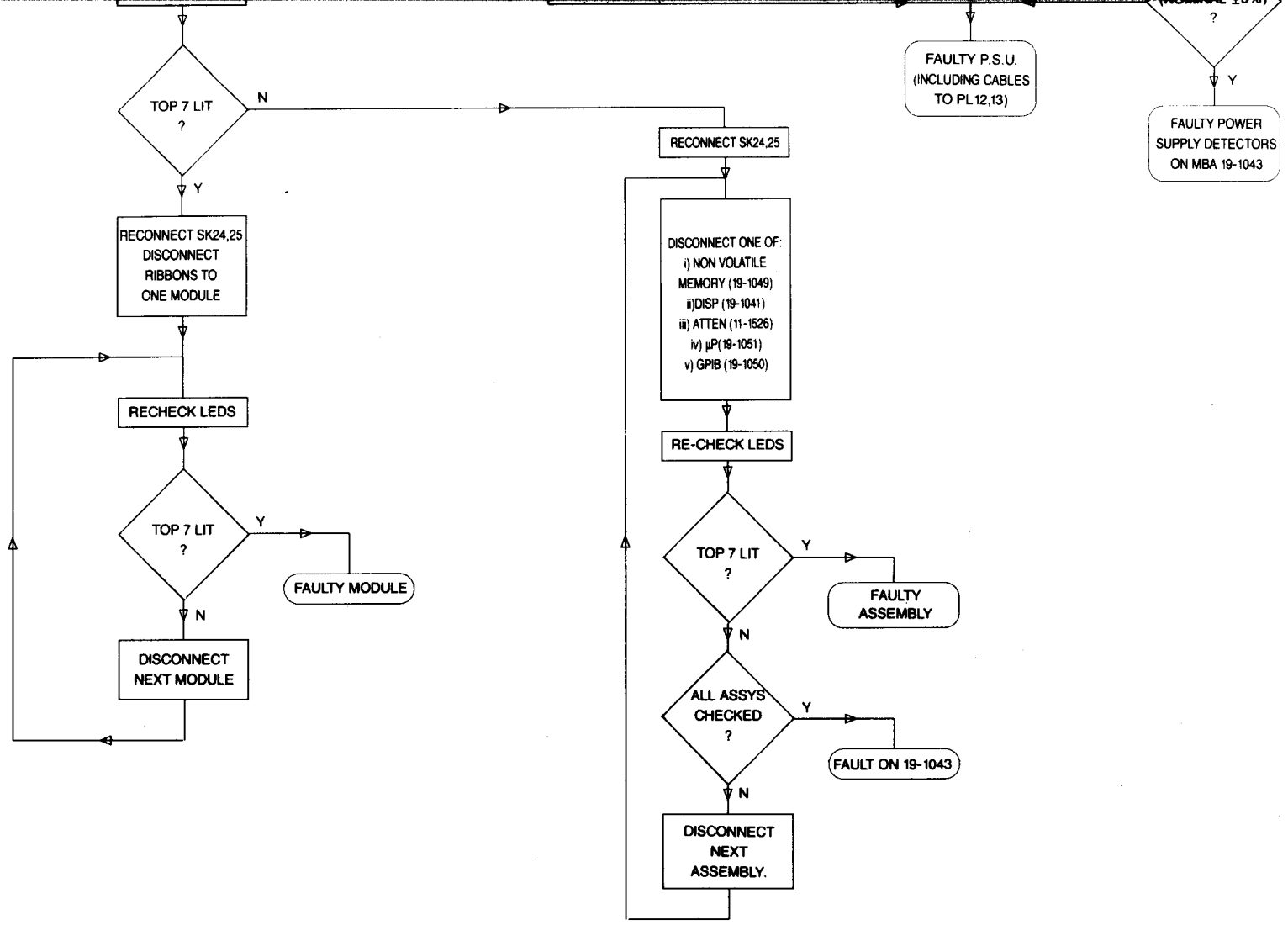


Fig. 7.8 Fault Finding P


FAULTY P.S.U.
(INCLUDING CABLES
TO PL12,13)
?
Y
FAULTY POWER
SUPPLY DETECTORS
ON MBA 19-1043
TOP 7 LIT
?
N
Y
RECONNECT SK24,25
DISCONNECT
RIBBONS TO
ONE MODULE
RECHECK LEDS
TOP 7 LIT
?
Y
FAULTY MODULE
N
DISCONNECT
NEXT MODULE
RECONNECT SK24,25
DISCONNECT ONE OF:
i) NON VOLATILE
MEMORY (19-1049)
ii)DISP (19-1041)
iii) ATTEN (11-1526)
iv) µP(19-1051)
v) GPIB (19-1050)
RE-CHECK LEDS
TOP 7 LIT
?
Y
FAULTY
ASSEMBLY
N
ALL ASSYS
CHECKED
?
Y
FAULT ON 19-1043
N
DISCONNECT
NEXT
ASSEMBLY.

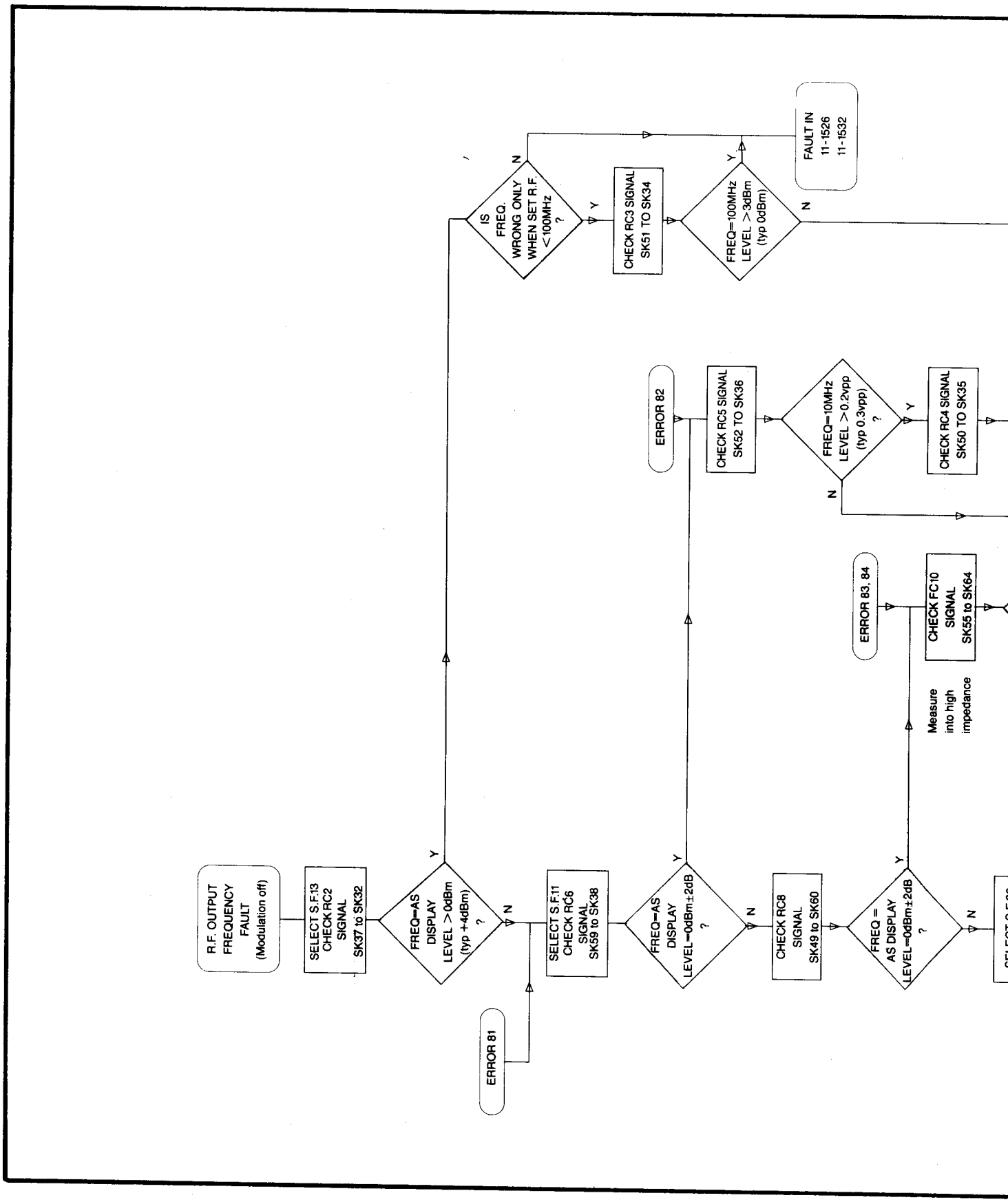
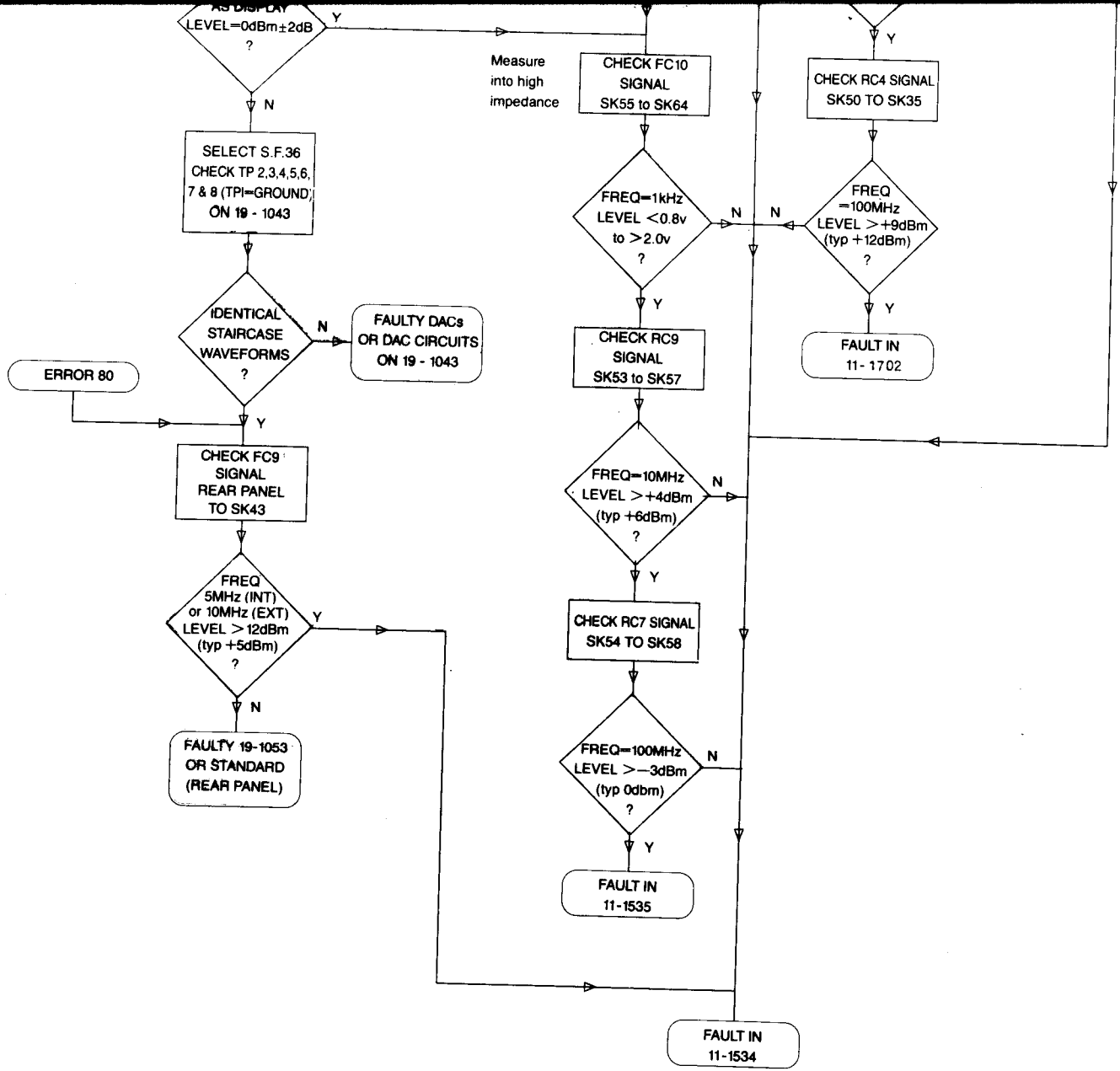


Fig. 7.9 Fault Finding P


AS DISPLAY
LEVEL=0dBm±2dB
?
Y
N
Measure into high impedance
SELECT S.F.36
CHECK TP 2,3,4,5,6, 7 & 8 (TP!=GROUND) ON 19 - 1043
IDENTICAL STAIRCASE WAVEFORMS
?
N
FAULTY DACs OR DAC CIRCUITS ON 19 - 1043
ERROR 80
Y
CHECK FC9 SIGNAL REAR PANEL TO SK43
FREQ 5MHz (INT) or 10MHz (EXT) LEVEL >12dBm (typ +5dBm)
?
Y
N
FAULTY 19-1053 OR STANDARD (REAR PANEL)
CHECK FC10 SIGNAL SK55 to SK64
FREQ=1kHz LEVEL <0.8v to >2.0v
?
N
Y
CHECK RC9 SIGNAL SK53 to SK57
FREQ=10MHz LEVEL >+4dBm (typ +6dBm)
?
N
Y
CHECK RC7 SIGNAL SK54 TO SK58
FREQ=100MHz LEVEL >−3dBm (typ 0dbm)
?
N
Y
FAULT IN 11-1535
FAULT IN 11-1534
Y
CHECK RC4 SIGNAL SK50 TO SK35
FREQ =100MHz LEVEL >+9dBm (typ +12dBm)
?
N
Y
FAULT IN 11-1702

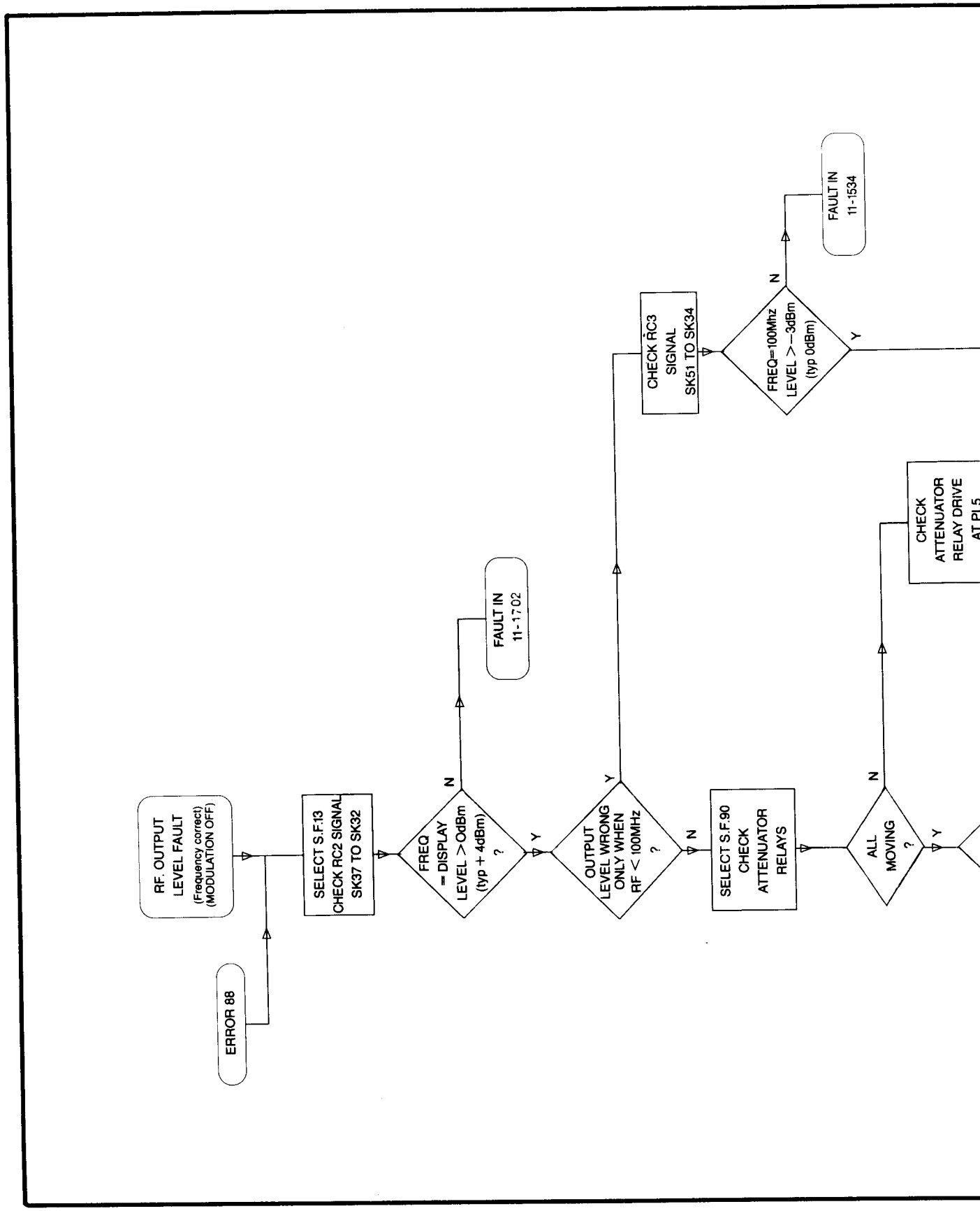
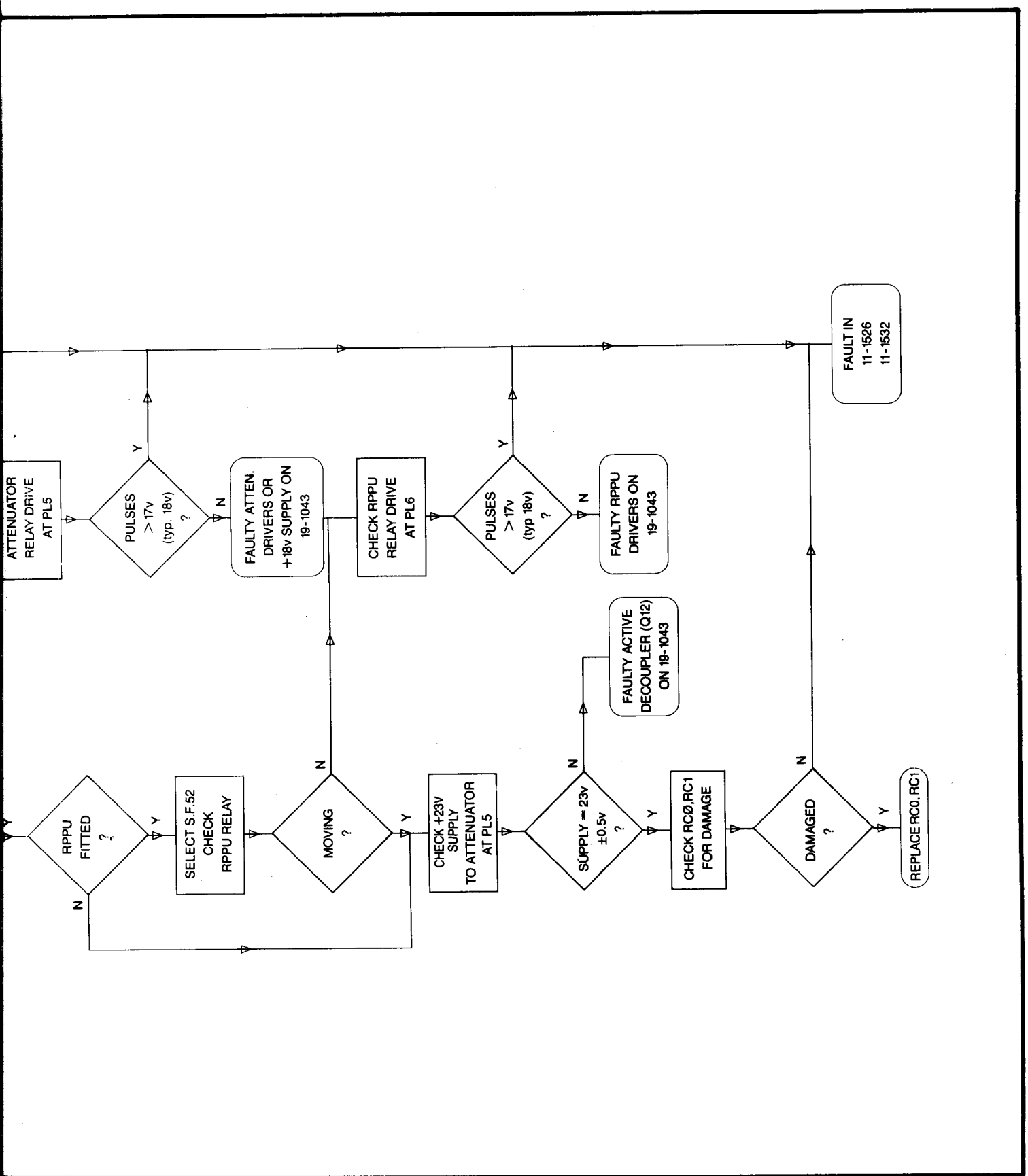


Fig. 7.10 Fault Fin



Finding Procedure - Chart D

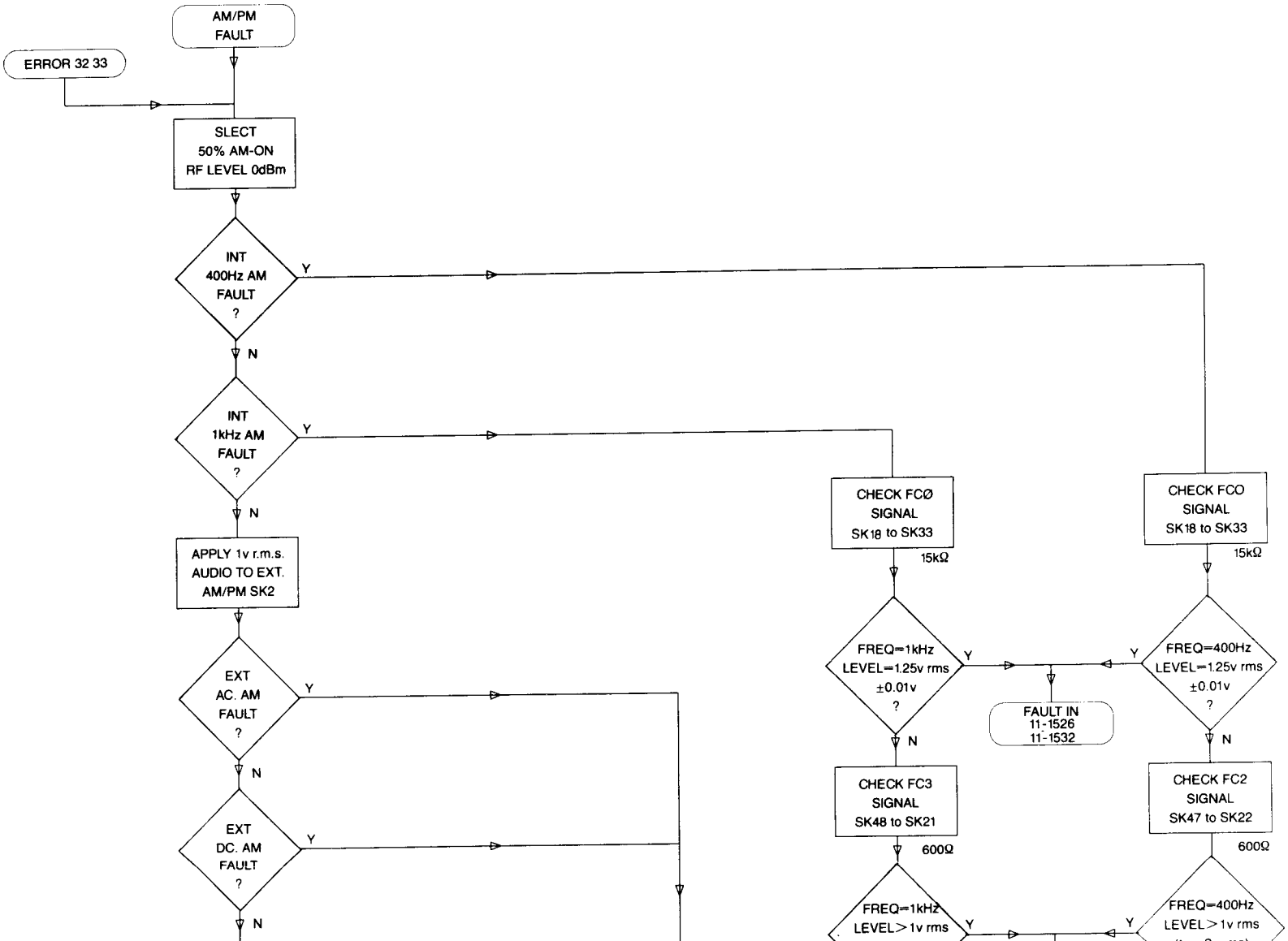
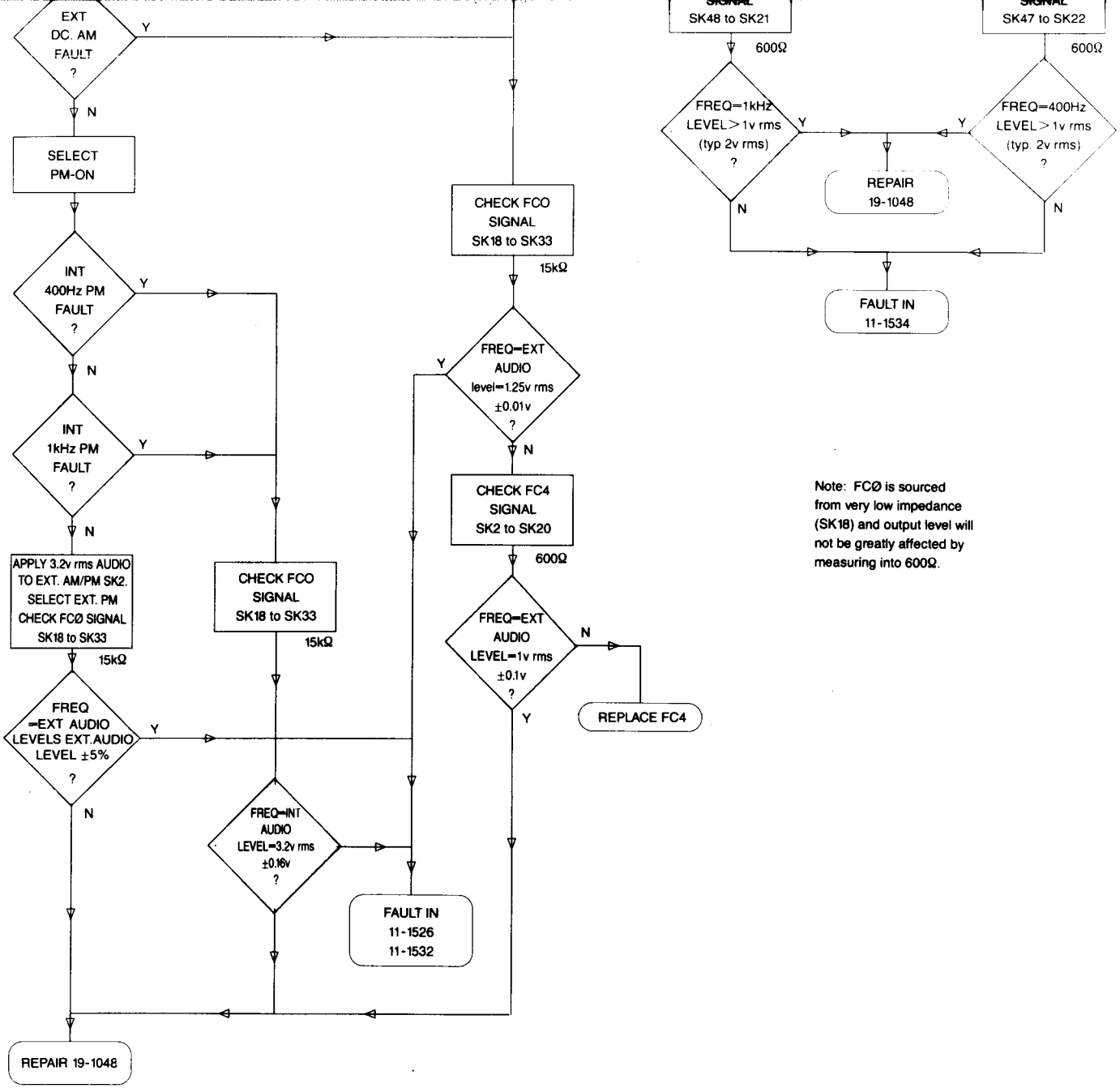


Fig. 7.11 Fault Finding



Note: FCØ is sourced from very low impedance (SK18) and output level will not be greatly affected by measuring into 600Ω.

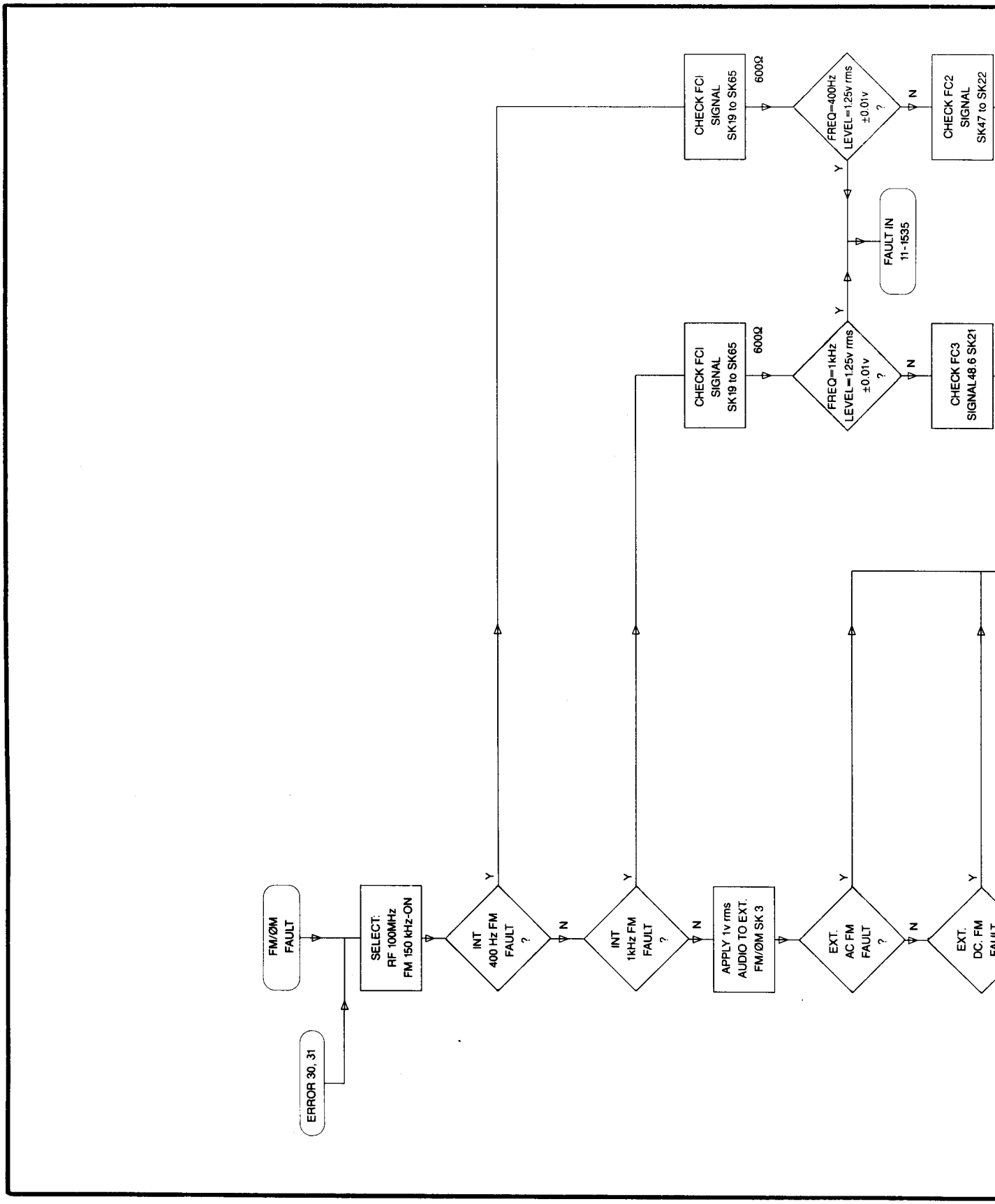
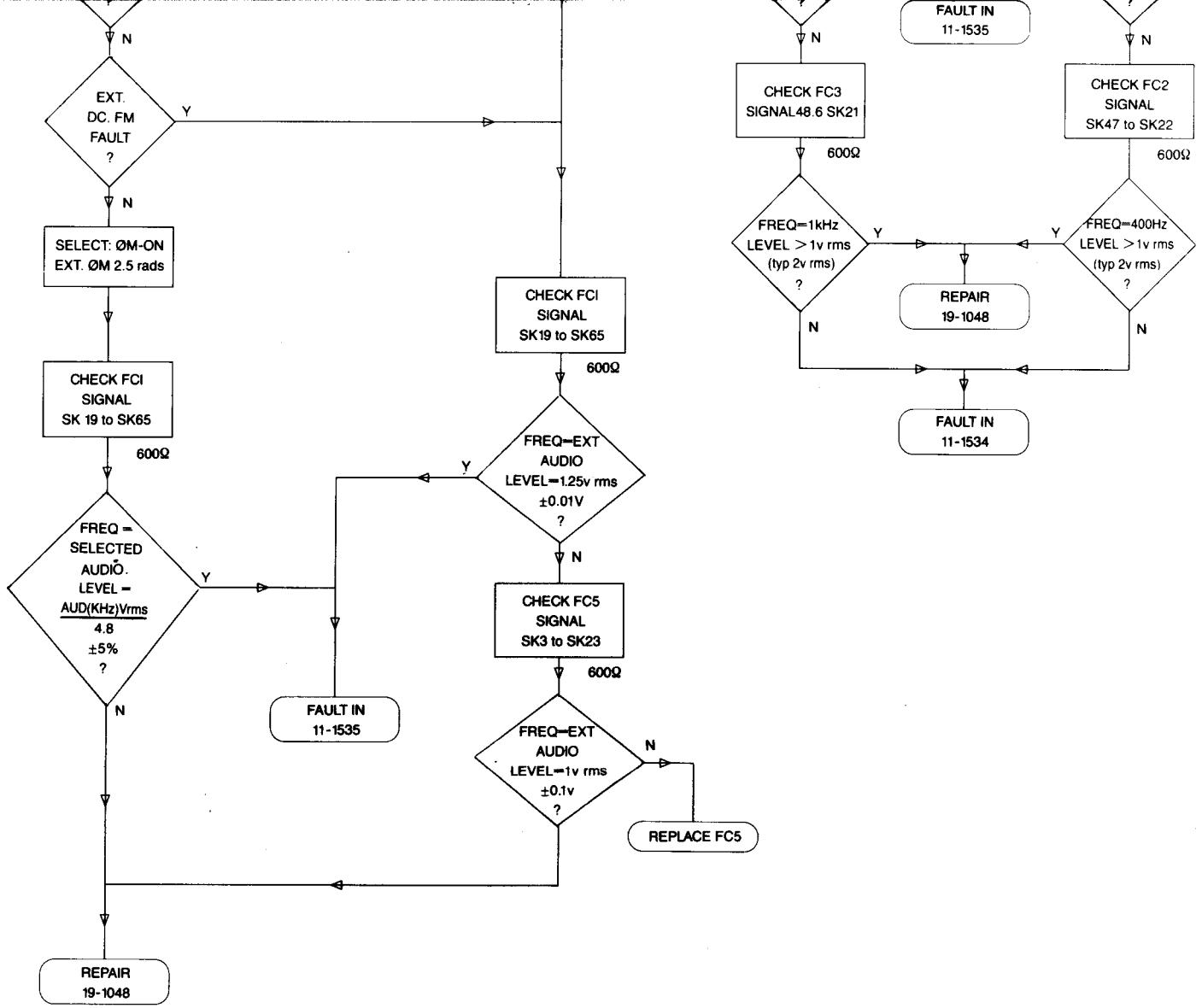


Fig 7.12 Fault Findin


N
EXT. DC. FM FAULT ?
Y
N
SELECT: ØM-ON EXT. ØM 2.5 rads
CHECK FCI SIGNAL SK 19 to SK65
600Ω
FREQ = SELECTED AUDIO. LEVEL = AUD(KHz)Vrms / 4.8 ±5% ?
Y
N
FAULT IN 11-1535
CHECK FCI SIGNAL SK19 to SK65
600Ω
FREQ=EXT AUDIO LEVEL=1.25v rms ±0.01V ?
Y
N
CHECK FC5 SIGNAL SK3 to SK23
600Ω
FREQ=EXT AUDIO LEVEL=1v rms ±0.1v ?
N
REPLACE FC5
REPAIR 19-1048
N
CHECK FC3 SIGNAL48.6 SK21
600Ω
FREQ=1kHz LEVEL > 1v rms (typ 2v rms) ?
Y
N
FAULT IN 11-1535
N
CHECK FC2 SIGNAL SK47 to SK22
600Ω
FREQ=400Hz LEVEL > 1v rms (typ 2v rms) ?
Y
N
REPAIR 19-1048
FAULT IN 11-1534

(c) Connect the frequency counter to measure the frequency at TP2 on assembly 19-1049.

(d) Check that the frequency counter indicates between 300 Hz and 366 Hz.

(e) Disconnect the frequency counter.

7.7.3.6 Option Check

7.7.3.6.1 Check LK1, between pins 1 and 2 on assembly 19-1049. The pins should be linked only when the 100-location store option is fitted.

7.7.3.6.2 Press the RECALL key. Turn the spinwheel clockwise and ensure that the memory display counts from 00 to the highest available memory location with no missed numbers. Ensure that the count stops at the highest available location number. Turn the spinwheel counterclockwise and check that the display counts back to 00.

7.7.3.7 Memory Corruption Check

7.7.3.7.1 Switch off the 9087 and remove assembly 19-1049 and the extender board. Fit assembly 19-1049 to the 9087. Switch on the 9087 and wait for the completion of the startup sequence. Activate special function 76. If memory corruption has occurred, an error message will be shown in the MEMORY display, but if not the instrument will return to the normal operating condition.

7.7.4 PROCESSOR ASSEMBLY 19-1051

7.7.4.1 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope	10
Extender Board 19-1123	21

7.7.4.2 Preparation for Testing

7.7.4.2.1 (a) Mount assembly 19-1051 on the extender board.

(b) Set R11 on assembly 19-1051 to its mid-position.

(c) Set the LBE, IBE and IRQ switches of S2 on assembly 19-1051 to the closed position, where the slider is towards the top of the board.

(d) Set the SIG ANAL, HALT, and NMI switches of S2 to the open position, where the slider is towards the bottom of the board.

(e) Disconnect the ribbon cables to assembly 19-1048 at PL24 and PL25.

7.7.4.3 Clock Timing Adjustment

7.7.4.3.1 Connect the oscilloscope to assembly 19-1051 as follows:

(a) Channel A input to TP9 using a X1 probe.

(b) Channel B input to TP7 using a X1 probe.

(c) Both probe ground connectors to TP3.

7.7.4.3.2 Set the oscilloscope time base to 100 ns/division (calibrated), externally triggered from the positive edge of the channel A input.

7.7.4.3.3 Switch on the 9087 and adjust the oscilloscope to obtain a display similar to Fig. 7.13. Adjust R11 until pulse width T is 370 ns ± 20 ns.

7.7.4.3.4 Switch off the 9087. Disconnect the oscilloscope and reconnect PL24 and PL25 on assembly 19-1048. Remove assembly 19-1051 and the extender board, and refit assembly 19-1051 to the 9087. Switch the 9087 on.

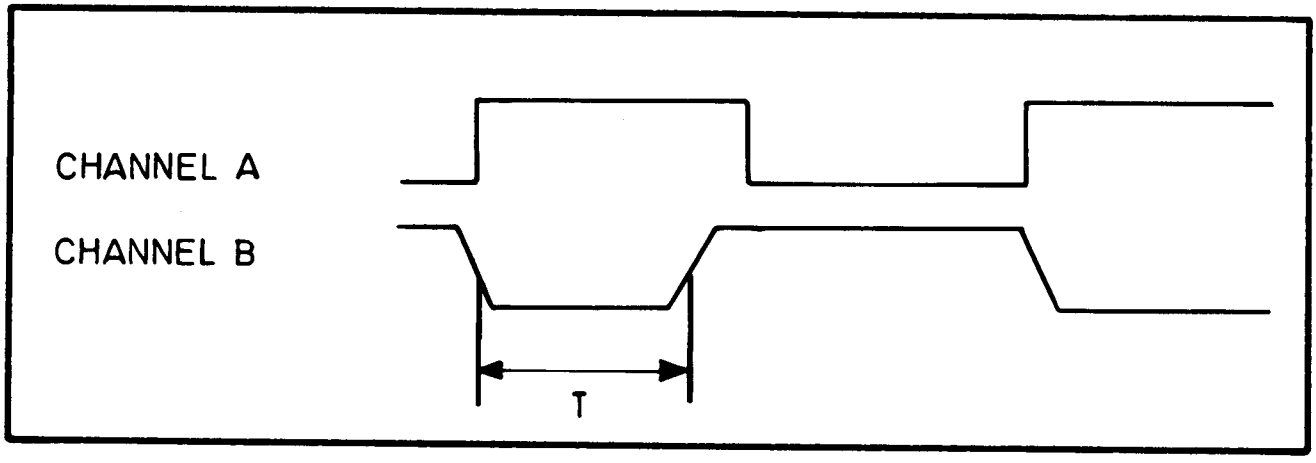


Fig. 7.13 Timing Adjustment Waveforms

7.7.4.4 NMI Test

7.7.4.4.1 Set the NMI switch of S2 on assembly 19-1051 to the closed position, where the slider is towards the top of the board. Check that the frequency display shows ---00000000---.

7.7.4.4.2 Operate the LOCAL key. Check that the modulation display shows 70 while the key is held pressed. Check that the frequency display shows ---00100000---.

7.7.4.4.3 Note the position of the spinwheel. Turn the spinwheel and check that the frequency display changes to ---00110000---. Return the spinwheel to its original position and check that the fourth digit reverts to 0.

7.7.4.4 Set the NMI switch to the open position, where the slider is towards the bottom of the board. Switch the 9087 off and on again.

7.7.4.5 Spinwheel Counter Test

7.7.4.5.1 Activate special function 27 and check that the frequency display shows +000. Using the spinwheel, check that the display can be varied from -128 to +127 with no missed numbers.

7.7.4.5.2 Operate the FREQUENCY key to cancel special function 27.

7.7.4.6 Standby Test

7.7.4.6.1 Operate the STANDBY key and check that all display elements except the STANDBY indicator are extinguished. Operate the STANDBY key and check that the 9087 returns to the operating condition.

7.7.5 MOTHERBOARD ASSEMBLY 19-1043

7.7.5.1 Test equipment required:

Item	Table 7.1 Item No.
Oscilloscope	10

7.7.5.2 Preparation for Testing

7.7.5.2.1 (a) Remove the module block.

(b) Remove assemblies 19-1049 (non-volatile memory) and 19-1050 (GPIB interface).

(c) Disconnect PL5 on the motherboard.

7.7.5.3 Out-of-Lock Lines Test

7.7.5.3.1 (a) Switch on the 9087. Check that the normal startup sequence is followed, except that the GPIB address is not displayed.

(b) Check that the 10^6 to 10^3 Hz digits flash, alternating between 0 and ····. An error indication should be given.

(c) Check that all four HIGH and LOW indicators adjacent to the external modulation inputs light.

(d) Activate special function 08. Check that 100.000000 is shown in the frequency display.

7.7.5.4 Spinwheel Test

7.7.5.4.1 Turn the spinwheel clockwise and counterclockwise. Check that the displayed frequency steps up and down correctly.

7.7.5.5 Keyboard Test

7.7.5.5.1 (a) Put the NMI switch of S2 on assembly 19-1051 to the closed position, where the slider is towards the top of the board.

(b) Check that the frequency display shows ····00000000····.

(c) Press each of the keys shown in Table 7.17 in turn and check that the corresponding key code appears in the amplitude display.

TABLE 7.17

Keyboard Check

Key	Code	Key	Code
LOCAL	70	kHz/µV	34
PULSE	61	COARSE	35
FM/ØM ON/OFF	52	RECALL	16
4	43	MEM EXCH	07

7.7.5.6 Setting the Monostable Timing

7.7.5.6.1 Activate special function 90. The frequency display will show the monostable pulse lengths, as shown in Fig. 7.14.

7.7.5.6.2 The clunker time is set by R59 on assembly 19-1043, and should be 5.0 ms. The attenuator pulse time is set by R21 on assembly 19-1043, and should be 40 ms. The attenuator delay time is nonadjustable, but should be between 380 ms and 660 ms.

7.7.5.6.3 Press the FREQUENCY key to cancel special function 90.

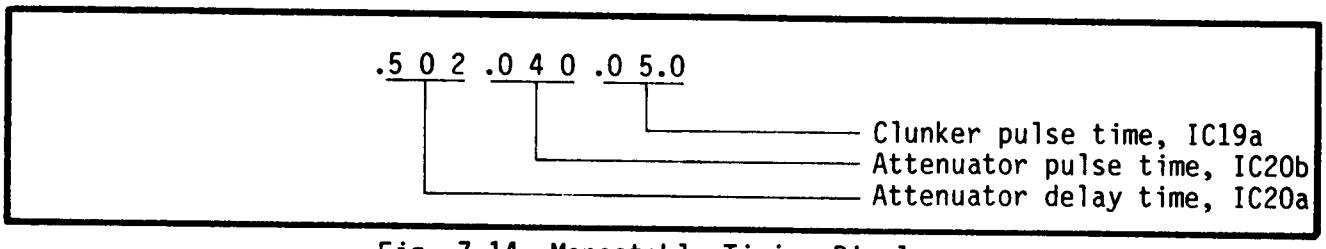


Fig. 7.14 Monostable Timing Display

7.7.5.7 Attenuator Drive Test

7.7.5.7.1 Connect the attenuator to the motherboard at PL5. Activate special function 90 and check that all the attenuator sections operate correctly.

7.7.5.7.2 Press any key to cancel special function 90.

7.7.5.8 Output Amplifier Control Test

7.7.5.8.1 Connect the oscilloscope to monitor the waveform at pin 14 of PL5 on assembly 19-1043. Activate special function 34 and check that the waveform shown in Fig. 7.15 is obtained. Disconnect the oscilloscope.

7.7.5.9 RPPU Circuit Test

7.7.5.9.1 Activate special function 52. The frequency display will show the pulse lengths of the RPPU drive monostables, as shown in Fig. 7.16.

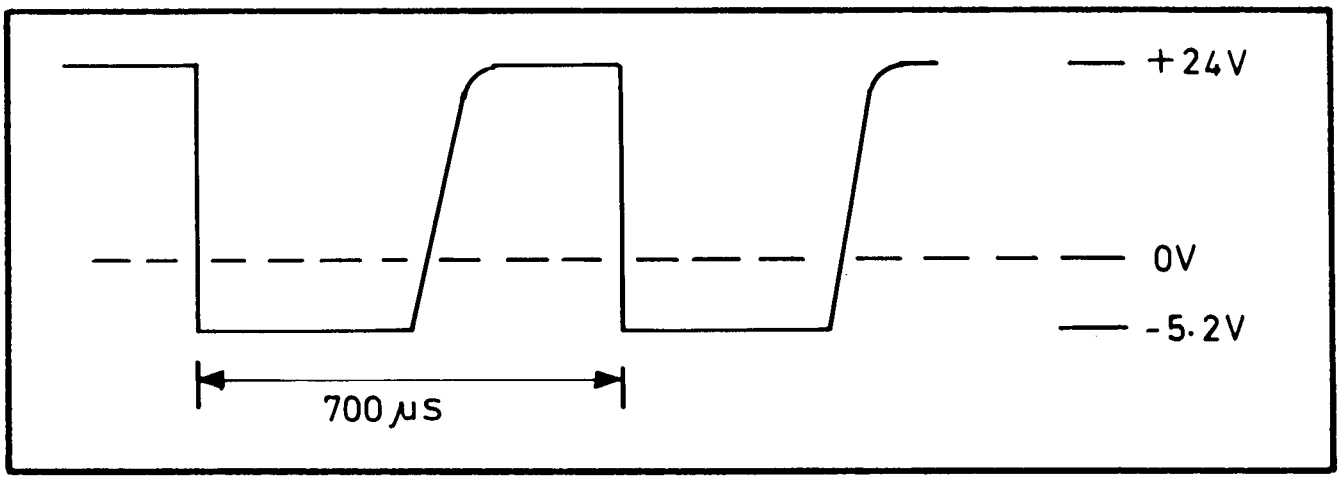


Fig. 7.15 Amplifier Control Waveform

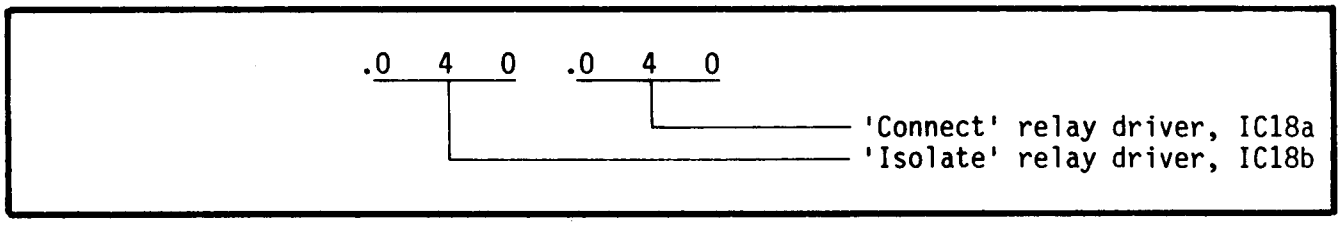


Fig. 7.16 Monostable Timing Display

7.7.5.9.2 Check that both measurements are between 35 ms and 55 ms, and that the RPPU relay (if fitted) operates correctly. Operate the FREQUENCY key to stop the timing check.

7.7.5.10 LF Synthesizer Drive

7.7.5.10.1 (a) Activate special function 36.

(b) Connect the ground lead of the oscilloscope probe to TP1 on assembly 19-1043.

(c) Monitor TP2 to TP8 in turn, and check that identical waveforms, similar to that shown in Fig. 7.17, occur at each test point.

(d) Operate the FREQUENCY key to cancel special function 36. Disconnect the oscilloscope.

7.7.5.11 Standby Test

7.7.5.11.1 Operate the STANDBY key. Check that the displays all blank except for the STANDBY indicator. Operate the STANDBY key a second time. Check that the displays return to normal with the STANDBY indicator extinguished.

7.7.5.12 GPIB And Memory Board Test

7.7.5.12.1 Switch off the 9087. Insert assembly 19-1050 and reconnect assembly 19-1053. Insert assembly 19-1049.

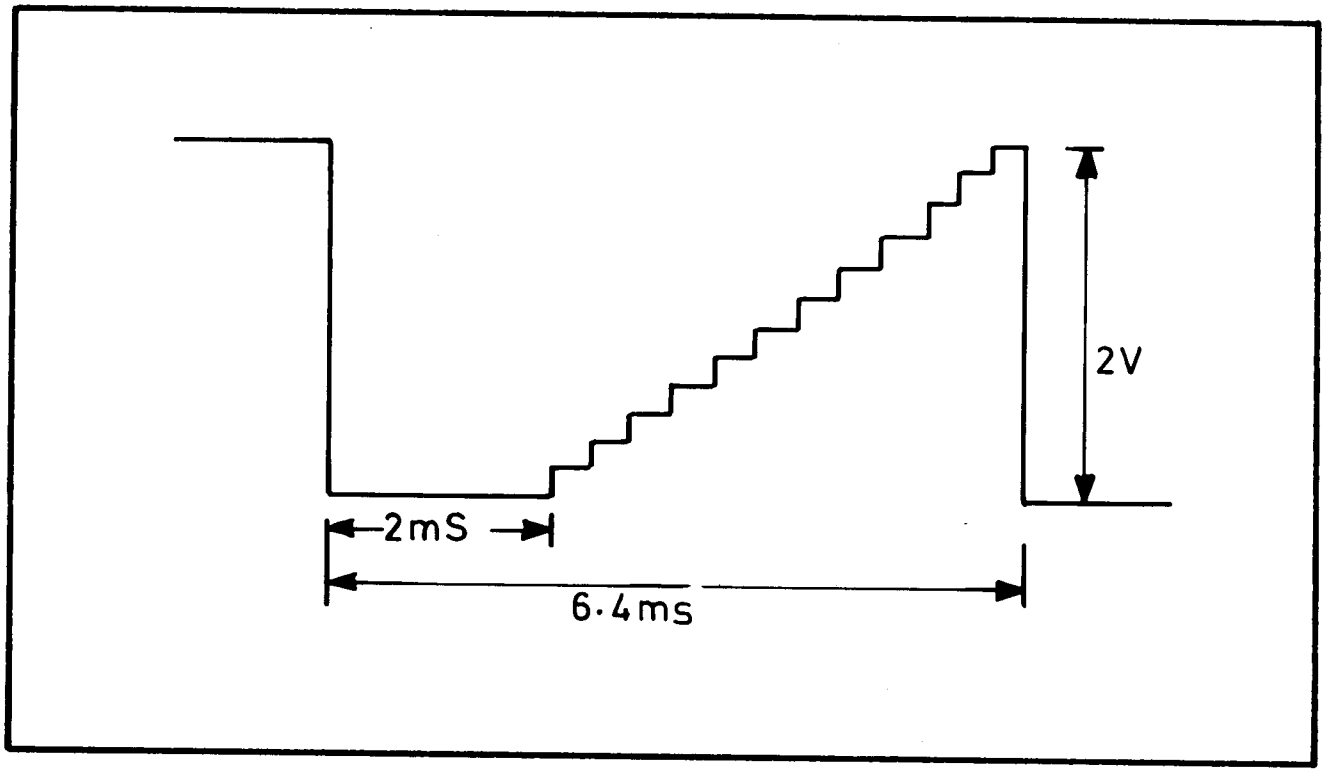


Fig. 7.17 D-to-A Converter Sweep Waveform

7.7.5.12.2 (a) Switch on the 9087. Check that the GPIB address is displayed during the startup sequence.

(b) Activate special function 21. Check that the frequency display shows the relevant pattern from Table 7.18.

TABLE 7.18

GPIB and Memory Board Test

Frequency Display	Assemblies Fitted
····11000000····	GPIB and 33 location memory.
····11000010····	GPIB, 33 location memory and RPPU.
····11100000····	GPIB and 100 location memory.
····11100010····	GPIB, 100 location memory and RPPU.

(c) Operate the FREQUENCY key to cancel special function 21.

(d) Turn the spinwheel to change the frequency. Note the frequency set.

(e) Switch the 9087 off and on again. Check that the frequency set is the same as that noted in (d).

7.7.6 FM MODULE 11-1535

7.7.6.1 Test equipment required:

Item	Table 7.1 Item No
Frequency Counter	2
Service Support Kit	21

7.7.6.2 Remove the module block from the 9087 and connect it to the main frame using the extender cables from the Service Support Kit.

7.7.6.3 Disconnect PL65 on module 11-1535. Disconnect PL56 and connect the frequency counter to measure the frequency at SK56.

7.7.6.4 (a) Switch on the 9087. Allow a minimum of 30 minutes warm-up time.

(b) Set a carrier frequency of 100 MHz. Select FM ON, EXT DC and peak deviation of 300 kHz.

(c) If necessary, adjust R3 on module 11-1535 to obtain a frequency counter indication of 100 MHz ± 0.001 MHz.

7.7.7 AUDIO SYSTEM ASSEMBLY 19-1048

7.7.7.1 Test equipment required:

Item	Table 7.1 Item No
Audio Signal Generator	6
True RMS Voltmeter	16
Distortion Analyzer	17

7.7.7.2 Preparation for Testing

7.7.7.2.1 The tests should be performed with assembly 19-1048 mounted on the module block in the 9087.

7.7.7.3 FM/ØM Channel

7.7.7.3.1 On assembly 19-1048, disconnect PL20, PL21 and PL22. Set R17, R57 and R78 to mid-position. Connect the signal generator to the FM AF IN socket. Connect the voltmeter to measure the AC signal at SK19.

7.7.7.3.2 Set the voltmeter input coupling to AC. Set the signal generator output to 1 kHz at a level of 1 V r.m.s. into 600 Ω.

7.7.7.3.3 (a) Switch on and initialize the 9087.

(b) Set the 9087 frequency to 600 MHz.

(c) Select FM, FM ON, and FM EXT DC.

(d) Set the peak deviation to 600 kHz.

(e) Adjust R18 on assembly 19-1048 to obtain a voltmeter indication of 2.5 V ± 0.01 V.

(f) Select FM EXT AC.

(g) Adjust R63 to obtain a voltmeter indication of 2.5 V ± 0.01 V.

(h) Disconnect PL23 and reconnect PL22. Select FM INT 400 Hz.

(j) Check that the voltmeter indicates 2.5 V ± 0.25 V.

(k) Disconnect PL22 and reconnect PL21. Select FM INT 1 kHz.

(l) Check that the voltmeter indicates 2.5 V ± 0.25 V.

7.7.7.3.4 Disconnect the test equipment. Reconnect PL20, PL22 and PL23. Connect the voltmeter to measure the DC level at IC11/6.

7.7.7.3.5 (a) Select FM EXT DC.

(b) Adjust R17 on assembly 19-1048 to obtain a voltmeter indication of 0 V ± 0.001 V.

(c) Transfer the voltmeter to measure the DC level at TP4.

(d) Adjust R78 to obtain a voltmeter indication of 0 V ± 0.001 V.

(e) Disconnect the test equipment.

7.7.7.3.6 Connect the signal generator to the FM AF IN socket. Connect the voltmeter to measure the AC signal at SK19. Set the signal generator output to 1 kHz at a level of 1 V r.m.s. into 600 Ω.

7.7.7.3.7 (a) Set the 9087 FM deviation to 300 kHz.

(b) Set the 9087 frequency to 300 MHz.

(c) Note the voltmeter indication.

(d) Change the 9087 frequency to 299 MHz.

(e) Adjust R57 to obtain a voltmeter indication within ±0.01 V of that obtained in (c).

(f) Repeat (b) to (e) until the voltmeter indications at 300 MHz and 299 MHz differ by less than 0.01 V.

7.7.7.3.8 (a) Initialize the 9087. Select ØM, ØM ON, and ØM EXT AC.

(b) Set the peak phase deviation to 2.5 radians.

(c) Adjust R82 on assembly 19-1048 to obtain a voltmeter indication of 0.208 V ± 0.001 V.

(d) Initialize the 9087. Select ØM, ØM ON and ØM EXT AC.

(e) Disconnect the signal generator.

(f) Set the voltmeter to measure mean DC level.

(g) Adjust R89 to obtain a voltmeter indication of 0 V ± 0.001 V.

7.7.7.3.9 Disconnect the voltmeter. Connect the signal generator to the FM AF IN socket. Connect the distortion analyzer to SK19. Set the signal generator output to 1 kHz at a level of 1 V r.m.s. into 600 Ω.

7.7.7.3.10 (a) Set the 9087 frequency to 600 MHz. Select FM, FM ON, and FM EXT AC.

(b) Set the FM deviation to 600 kHz.

(c) Check that the distortion measured at SK19 is less than 0.8%.

(d) Disconnect the distortion analyzer.

7.7.7.3.11 (a) Set the signal generator output to 1 kHz at a level of 0.195 V into 600 Ω.

(b) Adjust R36 on assembly 19-1048 until the FM LOW indicator lights.

(c) Turn R36 back to the point where the indicator just turns off.

(d) Decrease the signal generator output level to 0.19 V and check that the indicator lights.

(e) Increase the signal generator output level to 0.21 V and check that the indicator turns off.

(f) Increase the signal generator output level to 2.05 V.

(g) Adjust R35 until the FM HIGH indicator is off.

(h) Turn R35 back to the point where the indicator just turns on.

(j) Decrease the signal generator output to 1.9 V and check that the indicator is "off".

(k) Increase the signal generator output to 2.1 V and check that the indicator is "on".

(l) Disconnect all the test equipment.

7.7.7.4 AM/Pulse Channel

7.7.7.4.1 On assembly 19-1048, disconnect PL21, PL22 and PL23. Set R115 and R181 to mid-position. Connect the signal generator to the AM AF IN socket. Connect the voltmeter to measure the AC signal at SK18.

7.7.7.4.2 Set the voltmeter input coupling to AC. Set the signal generator output to 1 kHz at a level of 1 V r.m.s. into 600 Ω.

7.7.7.4.3 (a) Initialize the 9087.

(b) Select AM, AM ON, and AM EXT DC.

(c) Set the AM depth to 99%.

(d) Adjust R118 on assembly 19-1048 to obtain a voltmeter indication of 2.475 V ± 0.01 V.

(e) Select AM EXT AC.

(f) Adjust R166 to obtain an indication on the voltmeter of 2.475 V ± 0.01 V.

(g) Disconnect PL20 and reconnect PL22. Select AM INT 400 Hz.

(h) Check that the voltmeter indicates 2.475 V ± 0.25 V.

(j) Disconnect PL22 and reconnect PL21. Select AM INT 1 kHz.

(k) Check that the voltmeter indicates 2.475 V ± 0.25 V.

7.7.7.4.4 Disconnect the test equipment. Reconnect PL20. Connect the voltmeter to measure the DC level at IC6/6.

7.7.7.4.5 (a) Select AM EXT DC.

(b) Adjust R115 on assembly 19-1048 to obtain a voltmeter indication of 0 V ± 0.001 V.

(c) Transfer the voltmeter to measure the DC level at TP2.

(d) Adjust R181 to obtain a voltmeter indication of 0 V ± 0.001 V.

(e) Disconnect the test equipment.

7.7.7.4.6 Connect the signal generator directly to the voltmeter. Set the signal generator output to 1 kHz at a level giving a voltmeter indication of 1 V r.m.s. Transfer the voltmeter to measure the AC signal at SK18. Connect the signal generator to the AM AF IN socket.

7.7.7.4.7 (a) Select PULSE, PULSE ON, and PULSE EXT AC.

(b) Check that the voltmeter indicates 1 V ± 0.05 V.

7.7.7.4.8 Disconnect the voltmeter. Connect the distortion analyser to SK18.

7.7.7.4.9 (a) Initialize the 9087.

(b) Select AM, AM ON, and AM EXT AC.

(c) Set the modulation depth to 99%.

(d) Check that the distortion measured at SK18 is less than 0.8%.

(e) Disconnect the distortion analyzer.

7.7.7.4.10 (a) Set the signal generator output to 1 kHz at a level of 0.195 V into 600 Ω.

(b) Adjust R130 on assembly 19-1048 until the AM LOW indicator lights.

(c) Turn R130 back to the point where the indicator just turns off.

(d) Decrease the signal generator output level to 0.19 V and check that the indicator lights.

(e) Increase the signal generator output level to 0.21 V and check that the indicator turns off.

(f) Increase the signal generator output level to 2.05 V.

(g) Adjust R129 until the AM HIGH indicator is off.

(h) Turn R129 back to the point where the indicator just comes on.

(j) Set the signal generator output level to 1.9 V and check that the indicator is "off".

(k) Increase the signal generator output to 2.1 V and check that the indicator is "on".

7.7.7.4.11 Switch off and disconnect all test equipment. Reconnect PL22 and PL23.

7.8 DISMANTLING AND REASSEMBLY

7.8.1 INTRODUCTION

WARNING: LETHAL AC VOLTAGE IS EXPOSED WHEN THE INSTRUMENT IS CONNECTED TO THE AC SUPPLY WITH THE COVERS REMOVED. SWITCH THE INSTRUMENT OFF AND DISCONNECT THE SUPPLY SOCKET FROM THE REAR PANEL BEFORE CARRYING OUT ANY DISMANTLING OR REASSEMBLY OPERATION.

7.8.1.1 Semi-Rigid Coaxial Connectors

7.8.1.1.1 Many of the interconnections between modules of the RF system are made using semirigid coaxial connectors, RCØ to RC10. These connectors must not be subjected to unnecessary bending or twisting. When connecting or disconnecting the terminations, two wrenches should be used, one to hold the hexagonal shank and one to turn the securing nut. The nut should not be overtightened.

7.8.1.1.2 Suitable wrenches are supplied as part of the Customer Service Support Kit, Racal-Dana part number 11-1579

7.8.1.2 Ribbon Cable Connectors

7.8.1.2.1 The ribbon cable connectors should be disconnected by pressing the two locking clips outwards. When reconnecting, align the plug and socket carefully to avoid damage to the pins. Press the socket firmly onto the plug until the locking clips are in position over the ends of the socket.

7.8.1.3 Assembly Location

7.8.1.3.1 The location of the assemblies within the instrument is shown in Section 8 Fig. 1 and Fig. 2.

7.8.2 REMOVING THE COVERS

(a) Stand the instrument on its front handles. Remove the two screws from each of the corner assemblies at the rear of the instrument. Remove the corner assemblies.

(b) The covers can now be removed by sliding them towards the rear of the instrument. Note that removal of the corner assemblies also releases the side trim panels, which should either be removed or secured by replacement of the corner assemblies.

(c) Replace the covers in the reverse manner. Note that the straight, unfolded edge of the cover fits to the front of the instrument, and locates in a groove in the rear face of the front panel. The rear edge of the cover is folded, and fits over the edge of the rear panel.

(d) Refit the side trim panels, if removed, with the ventilation slots at the front of the instrument. Replace and secure the rear corner assemblies.

7.8.3 ASSEMBLIES 19-1049, 19-1050 and 10-1051

7.8.3.1 To remove assembly 19-1049, 10-1950 or 19-1051 proceed as follows:

(a) Remove the top cover of the instrument.

(b) If assembly 19-1050 is to be removed, disconnect the ribbon connector from the board at SK68.

(c) Remove the screw securing the retaining clip to the pillar between assemblies 19-1049 and 19-1050.

(d) Raise the inner, angled ends of the board extractors. This will lift the assembly in its guide slots sufficiently to free the edge connector from the motherboard.

(e) Lift the assembly out of the instrument. Ensure that the polarizing plugs are retained in the motherboard socket.

7.8.3.2 When replacing the assembly, ensure that the board extractors are in the lowered position before inserting the assembly in the guide slots. Press down on the extractors to reengage the edge connectors. Refit the retaining clip.

7.8.3.3. Ensure that the battery on assembly 19-1049 is not accidentally short circuited while the assembly is out of the instrument.

7.8.4 REMOVING THE MODULE BLOCK

7.8.4.1 Care must be exercised when removing the module block to avoid damage to the coaxial connectors. The following procedure should be used:

(a) Remove the top cover.

(b) Remove assemblies 19-1049, 19-1050 and 19-1051.

(c) Disconnect coaxial connectors PL20 and PL23 on assembly 19-1048.

(d) Disconnect SK28 and SK29 (semi-rigid coaxial connections to module 11-1532) at rear left-hand corner of the module block.

(e) Disconnect ribbon connectors PL24 and PL25 on assembly 19-1048.

(f) Remove the four screws securing the module block to the support pillars at the right-hand side of the block.

(g) Lift the right-hand side of the block, using the handle. Push the support lever, pivoted to the rear support pillar, fully under the module block.

(h) Disconnect coaxial connectors PL43, PL44, PL45, and PL46 at the right-hand rear of assembly 11-1534.

(j) Hold the right-hand side of the block up, using the handle, and withdraw the support lever. Lower the block gently to the horizontal position.

(k) Remove the four screws securing the bearing caps at the left-hand side of the module block.

(l) Lift the module block vertically, using the handles, to remove it from the instrument.

7.8.4.2 To replace the block use the reverse of the above procedure.

7.8.5 DISMANTLING THE MODULE BLOCK

7.8.5.1 Introduction

7.8.5.1.1 Once the block is removed from the instrument it is possible to remove any module, disturbing only the connections to that module. However, it will sometimes be found to be easier to dismantle the block up to the point where the required module is removed. The procedure given covers the complete dismantling of the block, beginning at the top with assembly 19-1048.

7.8.5.2 Audio System Assembly 19-1048

7.8.5.2.1 To remove the assembly proceed as follows:

(a) Disconnect PL18, PL19, PL21, and PL22.

(b) Disconnect the ribbon cables connected to SK26 and SK27 from all the modules.

(c) Remove the seven screws and crinkle washers retaining the assembly, and lift it from the top of the block.

7.8.5.2.2 To replace the assembly use the reverse of the above procedure.

7.8.5.3 Output System Module 11-1532

7.8.5.3.1 To remove the module proceed as follows:

(a) Remove assembly 19-1048.

(b) Disconnect PL32 and PL33.

(c) Remove the four screws and crinkle washers securing the module to the side plates of the block.

(d) Lift the module out of the block. Note that coaxial lead FCØ is still attached at SK33.

7.8.5.3.2 To replace the module use the reverse of the above procedure.

7.8.5.4 Comb Loop Module 11-1702

7.8.5.4.1 To remove the module proceed as follows:

(a) Remove assembly 19-1048 and module 11-1532. If paragraph 7.8.5.2.1 (c) is omitted, the two units can be removed as one item.

(b) Disconnect PL35, PL36 and PL38.

(c) Remove the four screws and crinkle washers securing the module to the side plates of the block.

(d) Lift the module out of the block. Take care not to damage the coaxial connectors. Note that coaxial connector RC2 is still attached to SK37.

7.8.5.4.2 To replace the module use the reverse of the above procedure.

7.8.5.5 Reference Generator and LF Synthesizer Module 11-1534

7.8.5.5.1 To remove the module proceed as follows:

(a) Remove assembly 19-1048, module 11-1532, and module 11-1702.

(b) Disconnect SK55.

(c) Disconnect SK49, SK53, and SK54. Access to SK49 is improved if SK61 is disconnected.

(d) Remove the four screws and crinkle washers securing the module to the sideplates of the block.

(e) Lift the module out of the block. Take care not to damage the coaxial connectors. Note that connectors RC3, RC4, RC5, RC8, FC2, and FC3 are attached to module 11-1534, and connectors RC6, RC7, RC9, RC10, FC1, and FC10 are attached to module 11-1535.

7.8.5.5.2 To replace the module use the reverse of the above procedure.

7.8.6 POWER SUPPLY CONTROL ASSEMBLY 19-1059

7.8.6.1 To remove assembly 19-1059 proceed as follows:

(a) Remove the two screws from the upper and lower left-hand corners of the hinged cover on the rear panel. Open the cover.

(b) Unscrew the two hexagonal pillars.

(c) Slide assembly 19-1059 to the left to disconnect PL71.

(d) Remove the assembly from the instrument.

7.8.6.2 To replace the assembly use the reverse of the above procedure.

7.8.7 POWER SUPPLY INTERCONNECT ASSEMBLY 19-1058

7.8.7.1 To gain access to the rear of assembly 19-1058 proceed as follows:

(a) Remove assembly 19-1059.

(b) Unsolder the leads from the thermistor to pins 10 and 11.

(c) Release the seven power transistors and two regulators from the heat sink.

(d) Remove the two screws securing the assembly. This allows the assembly to be raised at the right-hand side.

7.8.7.2 When refitting the power transistors and regulators to the heat sink, ensure that the insulating bushings and mica washers are correctly positioned.

7.8.8 GPIB CONNECTOR ASSEMBLY 19-1053

7.8.8.1 To remove assembly 19-1053 proceed as follows:

(a) Remove the top cover.

(b) Disconnect SK68 on assembly 19-1050.

(c) Remove the two screws adjacent to the oscillator adjustment apertures and the interface address switch on the rear panel.

(d) Remove the address switch plate, threading the ribbon cable through the aperture in the rear panel.

(e) Remove the two flat nuts securing the assembly to the plate.

7.8.8.2 To replace the assembly use the reverse of the above procedure.

7.8.9 REAR PANEL ASSEMBLY

7.8.9.1 To remove the rear panel assembly proceed as follows:

(a) Remove the top cover of the instrument and the module block.

(b) Disconnect SK9 at the center of the rear of assembly 19-1043.

(c) Disconnect SK68 at assembly 19-1050.

(d) Remove the four Taptite screws securing the rear panel to the side members of the instrument case.

CAUTION: DO NOT MIX TAPTITE SCREWS WITH MACHINE-THREADED SCREWS. TAPTITE SCREWS WILL DAMAGE THE THREADS OF ANY MACHINE-THREADED HOLES INTO WHICH THEY ARE INSERTED. MACHINE-THREADED SCREWS WILL NOT HOLD THE REAR PANEL SECURELY.

(e) Draw the rear panel away from the case to the limit of the power supply wiring. It may be necessary to feed the switch-wiring through the cable tie at the corner of the fan.

(f) Disconnect SK12 and SK13 at the rear right-hand corner of assembly 19-1043.

(g) If the rear panel is to be detached from the case, remove the screw holding the supply switch bracket and the screw holding the switch-operating button bracket.

7.8.9.2 Replace the panel using the reverse of the above procedure.

7.8.10 POWER SUPPLY CHASSIS ASSEMBLY

7.8.10.1 The layout of the components within the chassis is shown in Section 8 Fig. 17 of this manual. To gain access to the components proceed as follows:

(a) Remove assembly 19-1059.

(b) Remove the rear panel from the instrument to the limit of the wiring.

(c) Remove the five countersunk screws holding the chassis assembly to the rear panel. These are positioned above and below assembly 19-1058, and in the space previously covered by assembly 19-1059.

(d) Ease the power supply chassis away from the rear panel.

(e) If access to the components on the heatsink is required, remove the three screws securing the heatsink end of the chassis. The chassis end can then be folded back.

7.8.10.2 Reassemble the chassis using the reverse of the above procedure.

7.8.11 FREQUENCY STANDARD AND ASSEMBLY 19-1167

7.8.11.1 To remove the frequency standard proceed as follows:

(a) Remove the top cover of the instrument.

(b) Remove assembly 19-1053.

(c) Remove the two screws securing the frequency standard to the rear panel.

(d) Lift the frequency standard and assembly 19-1167 out of the instrument.

(e) Unsolder the frequency standard from assemby 19-1167 if required.

7.8.11.2 Replace the frequency standard and assembly 19-1167 using the reverse of the above procedure.

7.8.12 ATTENUATOR ASSEMBLY 11-1526

7.8.12.1 To remove the attenuator assembly proceed as follows:

(a) Remove the top and bottom covers.

(b) Remove the module block.

(c) Disconnect SK66 and SK67.

(d) Disconnect SK5 on assembly 19-1043.

(e) Remove the two screws securing the attenuator to the aluminum plate at the bottom of the instrument.

(f) Draw the attenuator into the instrument until the RF OUTPUT socket is clear of the front panel. Lift the attenuator out of the instrument.

7.8.12.2 Replace the attenuator using the reverse of the above procedure.

7.8.13 FRONT PANEL ASSEMBLY

7.8.13.1 To remove the front panel assembly proceed as follows:

(a) Remove the top cover and side trim panels.

(b) Remove the module block.

(c) Disconnect SK7 and SK8 at the front of assembly 19-1043.

(d) Remove the two screws securing the handle at each side of the instrument.

(e) Remove the eight Taptite screws holding the front panel to the side members of the instrument case.

CAUTION: DO NOT MIX TAPTITE SCREWS WITH MACHINE-THREADED SCREWS. TAPTITE SCREWS WILL DAMAGE THE THREADS OF ANY MACHINE-THREADED HOLE INTO WHICH THEY ARE INSERTED. MACHINE-THREADED SCREWS WILL NOT HOLD THE FRONT PANEL SECURELY.

(f) Remove the front panel assembly.

7.8.13.2 Replace the front panel assembly using the reverse of the above procedure.

7.8.14 DISPLAY ASSEMBLY 19-1041

7.8.14.1 To gain access to the front of the display assembly proceed as follows:

(a) Remove the front panel assembly.

(b) Remove the two screws securing the spinwheel disc.

(c) Remove the fourteen flat nuts and crinkle washers securing assembly 19-1041 to the front panel.

(d) Ease the assembly away from the front panel, threading the coaxial leads through the holes, to the extent of the clunker leads. Note that the spacers on the front-panel studs are loose.

7.8.14.2 Refit the assembly using the reverse of the above procedure.

7.8.15 MOTHERBOARD ASSEMBLY 19-1043

7.8.15.1 To remove the assembly proceed as follows:

(a) Remove the top and bottom covers.

(b) Remove the module block.

(c) Disconnect SK5, SK7, SK8, SK9, SK12, and SK13 on assembly 19-1043.

(d) Disconnect SK66 and SK67 on assembly 11-1526.

(e) Invert the instrument chassis, and position it with the front panel to the left.

(f) Remove the six screws securing the aluminum plate to the sides of the instrument case.

(g) Lift the aluminum plate at the near edge (left-hand side of the instrument) and lift the plate and assembly 19-1043 clear of the chassis.

(h) Remove the twelve screws securing assembly 19-1043 to the aluminum plate.

7.8.15.2 Replace the assembly using the reverse of the above procedure.

7.9 OVERALL SPECIFICATION CHECK

7.9.1 INTRODUCTION

7.9.1.1 Satisfactory completion of the following performance verification procedures (PVPs) will confirm that the Model 9087, Synthesized Signal Generator, is fully functional and meets the specification. No accessing of the internal connections of the 9087 is required in conducting the PVPs.

7.9.1.2 Is is suggested that the results of these PVPs be retained for reference, so the PVPs have been presented, when possible, in tabular form. The tables are given on Pages 7-71 to 7-81 . These pages can be copied, if required, to provide a separate record of results.

7.9.1.3 The user should be aware of the following precautions prior to conducting any PVP:

(a) Line voltages must be within the required range stated on the rear panel of the 9087.

(b) The 9087 must have been switched on for not less than one hour.

(c) For the level accuracy tests, the ambient temperature must be $23^{o}C \pm 5^{o}C$.

7.9.1.4 For certain PVPs a preferred and an alternative method of testing are given. The preferred methods are given in paragraph 7.9.2, and the alternative methods in paragraph 7.9.3.

7.9.2 PREFERRED PVPs

7.9.2.1 Frequency PVP

7.9.2.1.1 Test equipment required:

Item	Table 7.1 Item No.
Frequency Counter	2
Frequency Distribution System	13

7.9.2.1.2 This frequency PVP confirms that all the phase-locked loops in the 9087 are operating properly. Use the following series of steps to complete the required frequency verification on the 9087:

(a) Initialize the 9087.

(b) Set the amplitude to -10 dBm.

(c) Connect the test equipment as shown in Fig. 7.18. Switch the 9087 to external standard.

(d) Select the frequencies shown in Table 7.19 and verify that the counter agrees within ± 1 Hz.

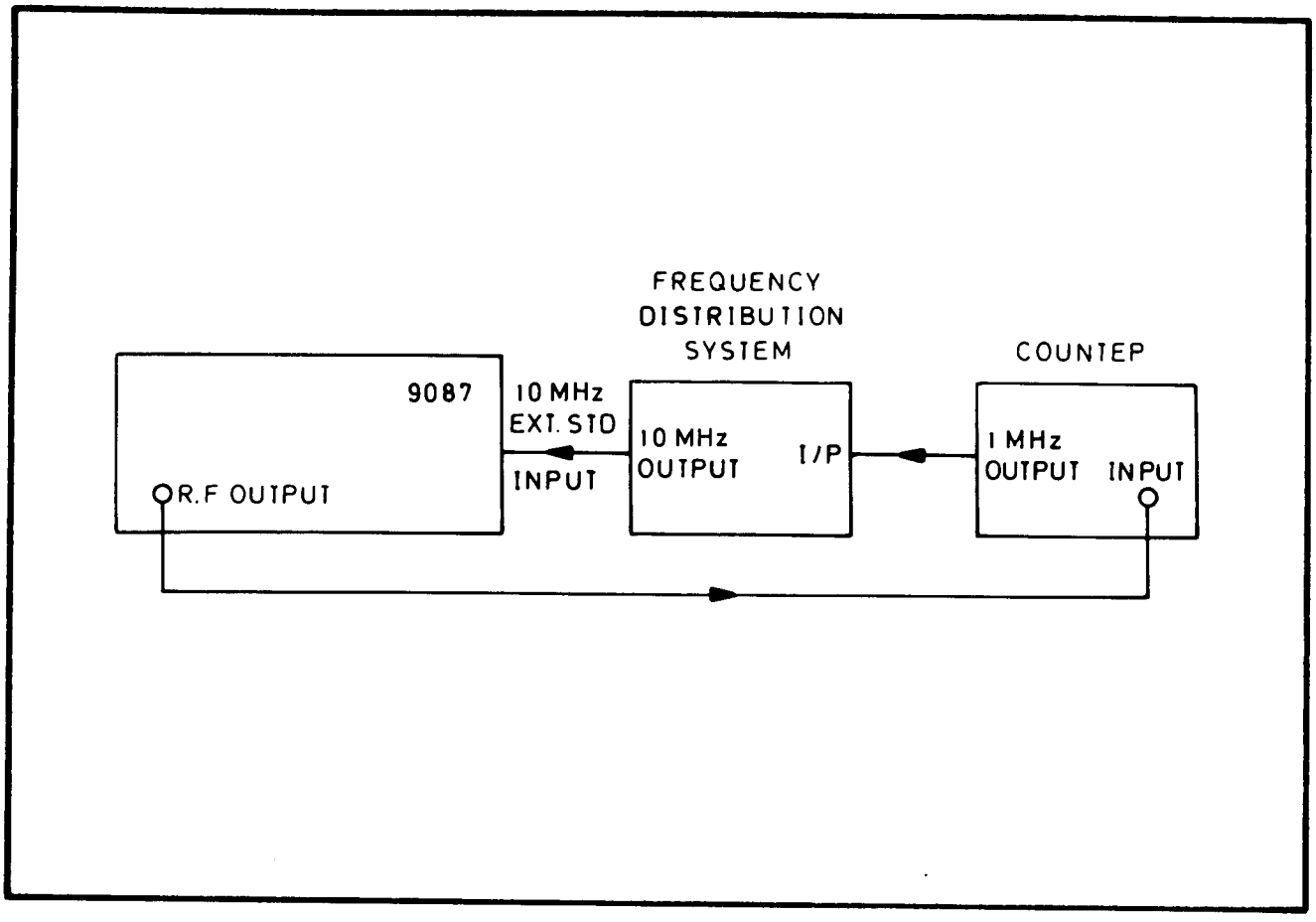


Fig. 7.18 Connections for Frequency PVP

7.9.2.2 Output Level Accuracy and Flatness PVP

7.9.2.2.1 Test equipment required:

Item	Table 7.1 Item No
Measuring Receiver	3

7.9.2.2.2 Use the following series of steps to complete the required output level accuracy verifications on the 9087:

(a) Zero the receiver.

(b) Attach the measuring receiver to the RF Output of the 9087 as shown in Fig. 7.19.

(c) Set the 9087 to the desired output level and frequency.

(d) Enter the power sensor calibration factor for each frequency setting.

(e) Record the measured output level at the settings given in Table 7.20.

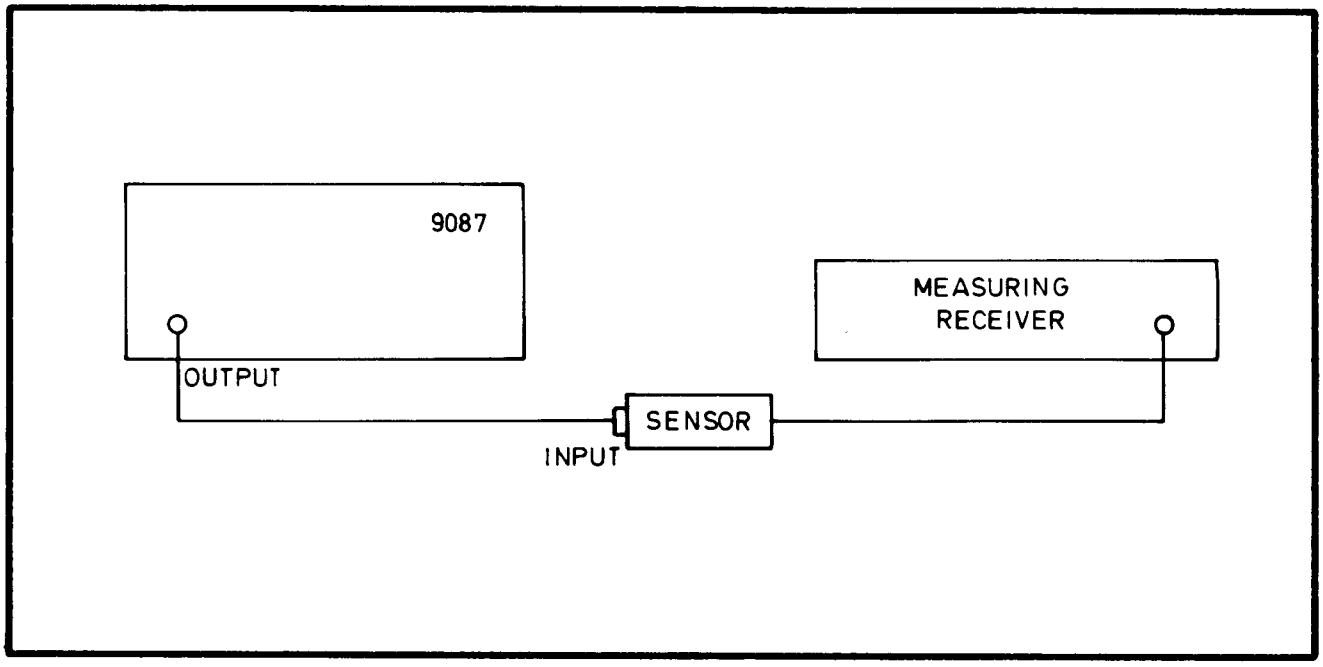


Fig. 7.19. Connections for Output Level PVP

7.9.2.2.3 The output level flatness is derived from the results tabulated for the output level accuracy at +13 dBm as follows:

(a) At frequencies below 650 MHz, the maximum deviation from the 400 MHz value should not be greater than ± 0.4 dB.

(b) At frequencies above 650 MHz, the maximum deviation from the 400 MHz value should not be greater than ± 0.7 dB.

(c) Indicate the corresponding correct output level flatness achieved in the appropriate box provided.

7.9.2.3 Attenuator PVP

7.9.2.3.1 Test equipment required:

Item	Table 7.1 Item No
Measuring Receiver	3

7.9.2.3.2 Use the following series of steps to complete the attenuator verification:

(a) Initialize the 9087.

(b) Connect the measuring receiver to the 9087 as shown in Fig. 7.20.

(c) Check the instructions for use of the receiver, if necessary.

(d) Execute the measurements shown in Table 7.21 using the relative mode of the receiver.

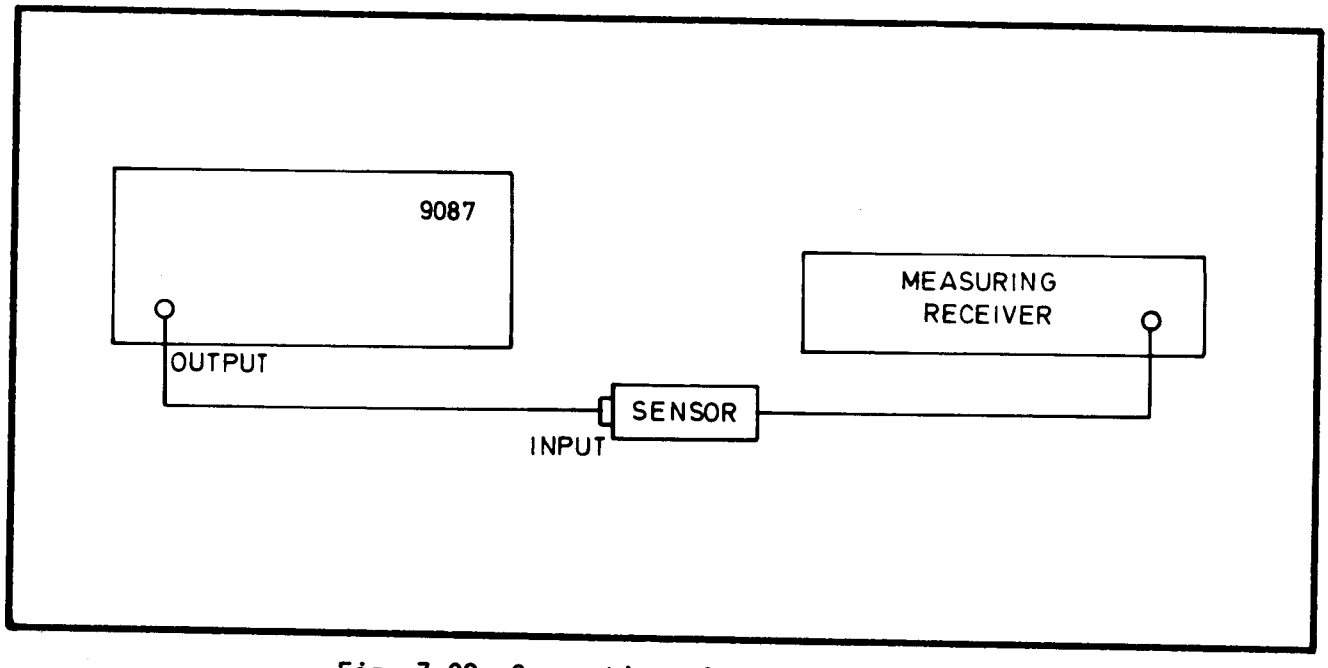


Fig. 7.20 Connections for Attenuator PVP

7.9.2.4 Audio Output PVP

7.9.2.4.1 Test equipment required:

Item	Table 7.1 Item No
Audio Analyzer	5
Frequency Counter	2
Frequency Distribution System	13

7.9.2.4.2 Connect the test equipment as shown in Fig. 7.21.

7.9.2.4.3 Use the following series of steps to complete the procedure for frequency verification:

(a) Connect the 400 Hz output from the 9087 to the Channel A input on the counter, with the counter set to measure frequency A with 0.1 Hz resolution.

(b) Connect the 10 MHz standard output from the 9087 to the external standard input on the frequency meter via the frequency distribution system. Set the frequency meter selector to EXTERNAL.

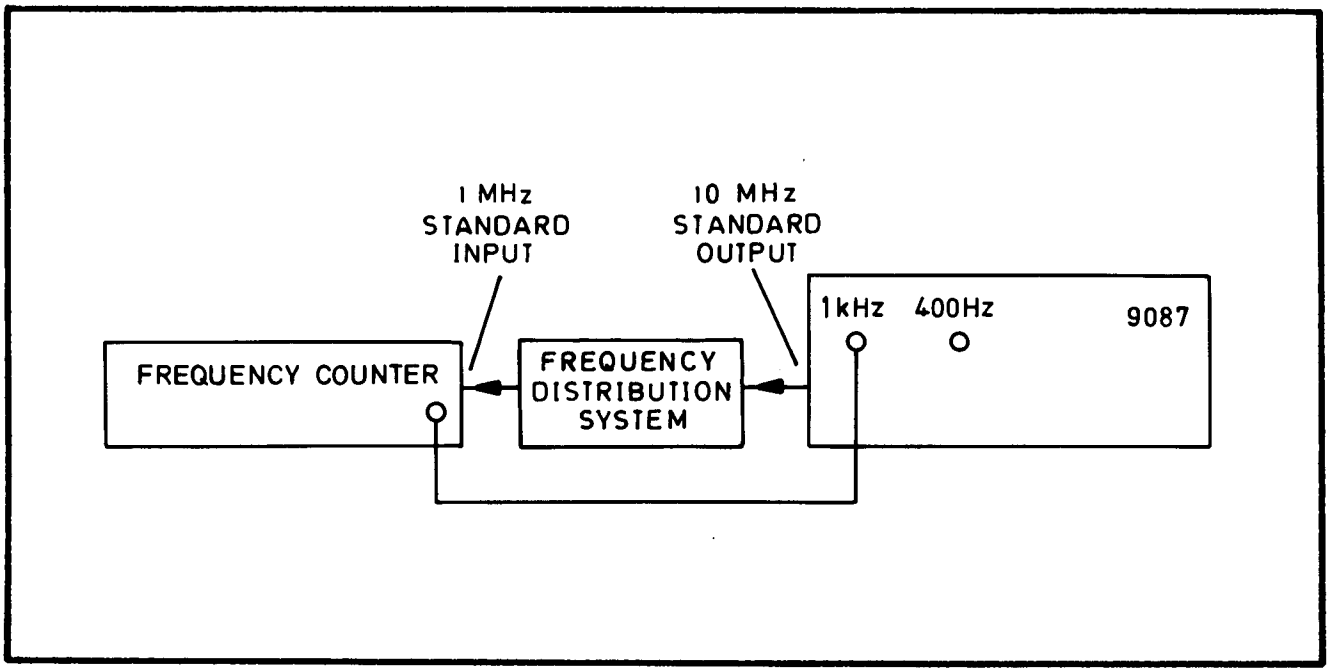


Fig. 7.21. Connections for Audio Output Frequency PVP

(c) Record the frequency in Table 7.22.

(d) Connect the 1 kHz output from the 9087 as described in step (a) and measure/record the frequency.

NOTE: This PVP confirms that the frequency synthesis capability of the 9087 is functioning properly. The frequency accuracy will then be the same as for the reference oscillator and will be determined in paragraph 7.9.2.9 on the internal standard.

7.9.2.4.4 Connect the test equipment as shown in Fig. 7.22.

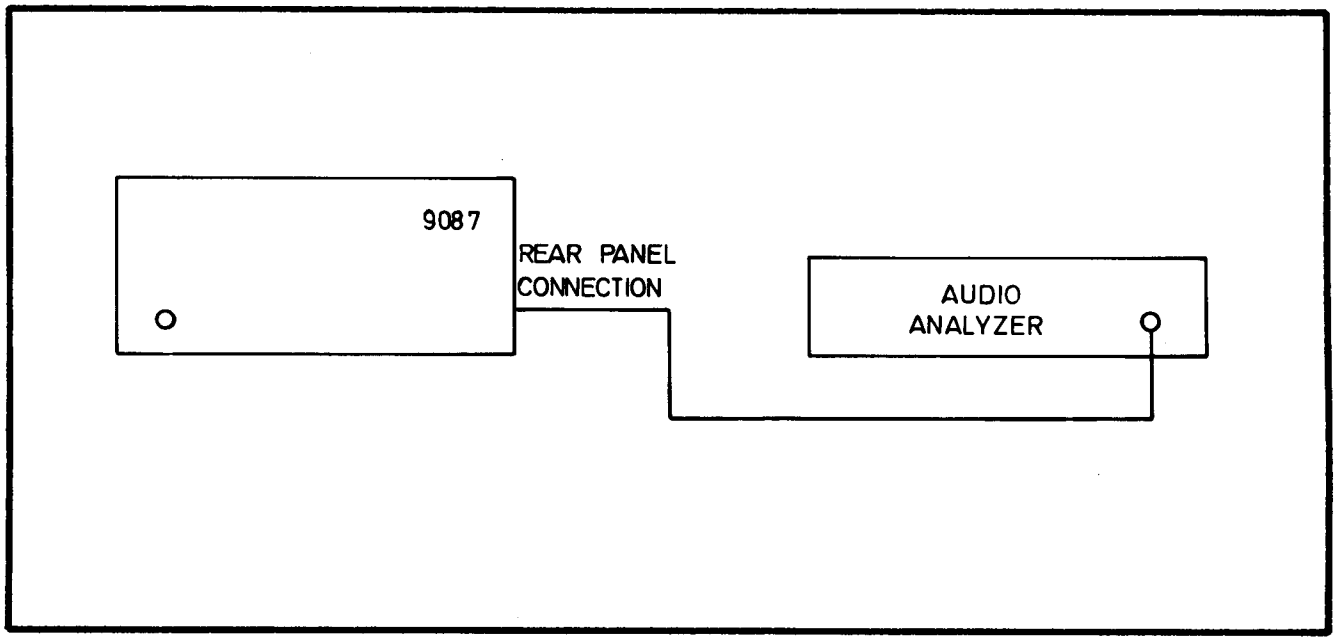


Fig. 7.22. Connections for Audio Output Level and Distortion PVP

7.9.2.4.5 Use the following series of steps to complete the audio output level and distortion verifications:

(a) Switch in the 30 kHz lowpass filter on the audio analyzer.

(b) Switch the analyzer to measure AC volts.

(c) Measure the audio output voltage and record the measurement in Table 7.23.

(d) Switch the analyzer to measure distortion.

(e) Measure the distortion and record the measurement in Table 7.23.

(f) Connect the analyzer to the 1 kHz audio output of the 9087.

(g) Repeat (b) to (c).

7.9.2.5 Modulation PVPs

7.9.2.5.1 Test equipment required:

Item	Table 7.1 Item No
Measuring Receiver	3
Audio Signal Generator	6
Frequency Counter	2
Spectrum Analyzer	14
DC Supply	8

7.9.2.5.2 Connect the test equipment as shown in Fig. 7.23.

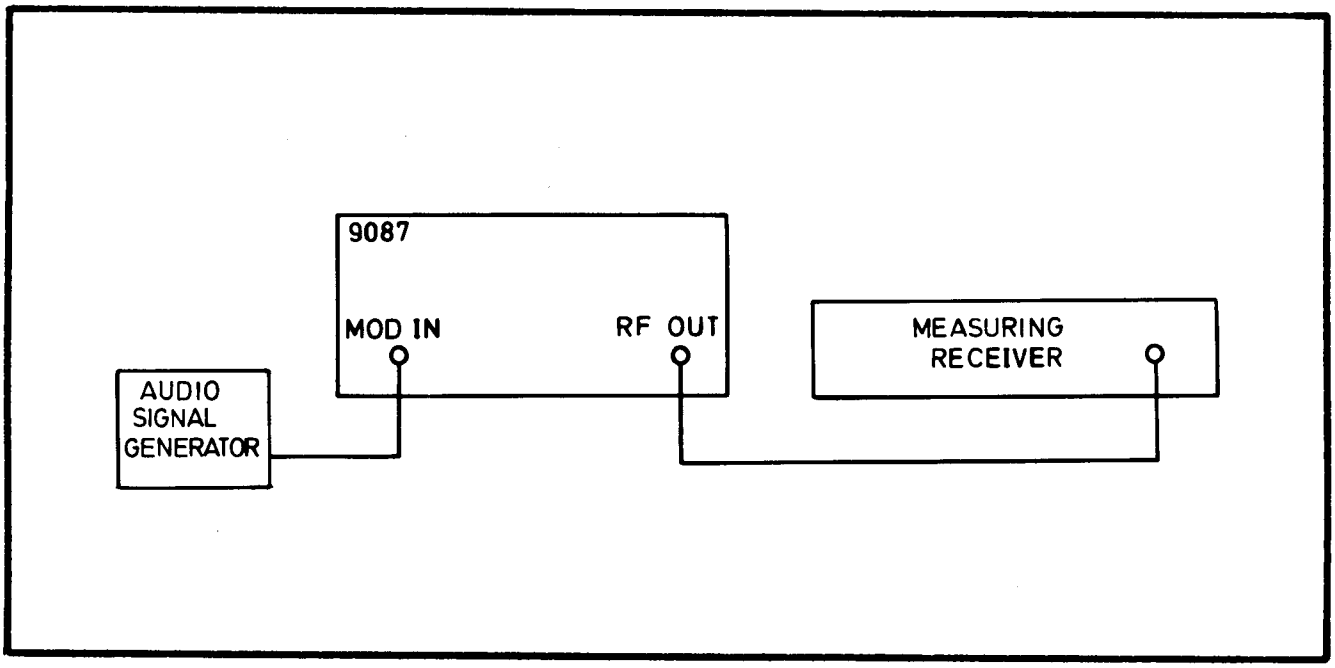


Fig. 7.23. Connections for Modulation PVP

7.9.2.5.3 Use the following series of steps to complete the internal frequency modulation verification.

(a) Set the 9087 to +3 dBm with the carrier frequency, modulation frequency, and deviation settings shown in Table 7.24

(b) Verify the deviation and % distortion and record the measurements in Table 7.24

7.9.2.5.4 Use the following series of steps to complete the high/low limit detector verification:

(a) Connect the audio signal to the FM/ØM socket on the 9087's front panel. Select EXT AC.

(b) Set the audio generator to a modulation frequency of 1 kHz.

(c) Vary the signal level of the audio generator from 0 to 2.2 V r.m.s. p.d.

(d) Check and record that the audio input high/low detector LEDs light as shown in Table 7.25.

(e) Repeat steps (a) to (d) for the AM/PULSE input.

7.9.2.5.5 Use the following series of steps to complete the external frequency modulation verification:

(a) Connect audio generator to FM/ØM socket on front panel. Select FM EXT AC.

(b) Set the audio generator level to 1 V r.m.s. p.d.

(c) Verify the deviation measurements and record the measurements in Table 7.26.

(d) Disconnect the audio generator from the FM/ØM socket. Connect the frequency counter to monitor the RF output of the 9087.

(e) Set the 9087 carrier frequency to 100 MHz.

(f) Select FM EXT DC, FM OFF, and peak deviation of 300 kHz.

(g) Note the frequency counter indication.

(h) Select FM ON and again note the frequency counter indication.

(j) The frequency change should not be more than ± 6250 Hz. If it is set up the DC FM center frequency as instructed in paragraph 7.7.6. Record the final frequency offset in the box provided below Table 7.26.

7.9.2.5.6 Use the following steps to complete the phase modulation verification:

(a) Set the 9087 to 1 kHz INT phase modulation, 5 radians deviation at a carrier frequency of 1300 MHz.

(b) Measure and record in Table 7.27 the deviation and distortion values.

(c) Set the 9087 to External AC phase modulation.

(d) With the audio generator connected to the FM/Phase Modulation Input and set to 10 kHz at 1 V r.m.s. p.d., measure and record in Table 7.28 the deviation values.

7.9.2.5.7 Use the following series of steps to complete the amplitude modulation verification:

(a) Set the 9087 to the +13 dBm output level, 1 kHz internal amplitude modulation and modulation depths of 80% and 30%.

(b) Verify the modulation and distortion, and record the measurements for the 80% and 30% modulation depths in Tables 7.29 and 7.30 respectively.

(c) Set the 9087 to External AC amplitude modulation, 80% modulation depth, with a carrier frequency of 1300 MHz.

(d) With the audio generator connected to the AM/Pulse modulation input and an output level of 1 V r.m.s. p.d. measure, and record in Table 7.31, the modulation depth, obtained for modulation frequencies of 1 kHz and 20 kHz.

7.9.2.5.8 Connect the test equipment as shown in Fig. 7.24.

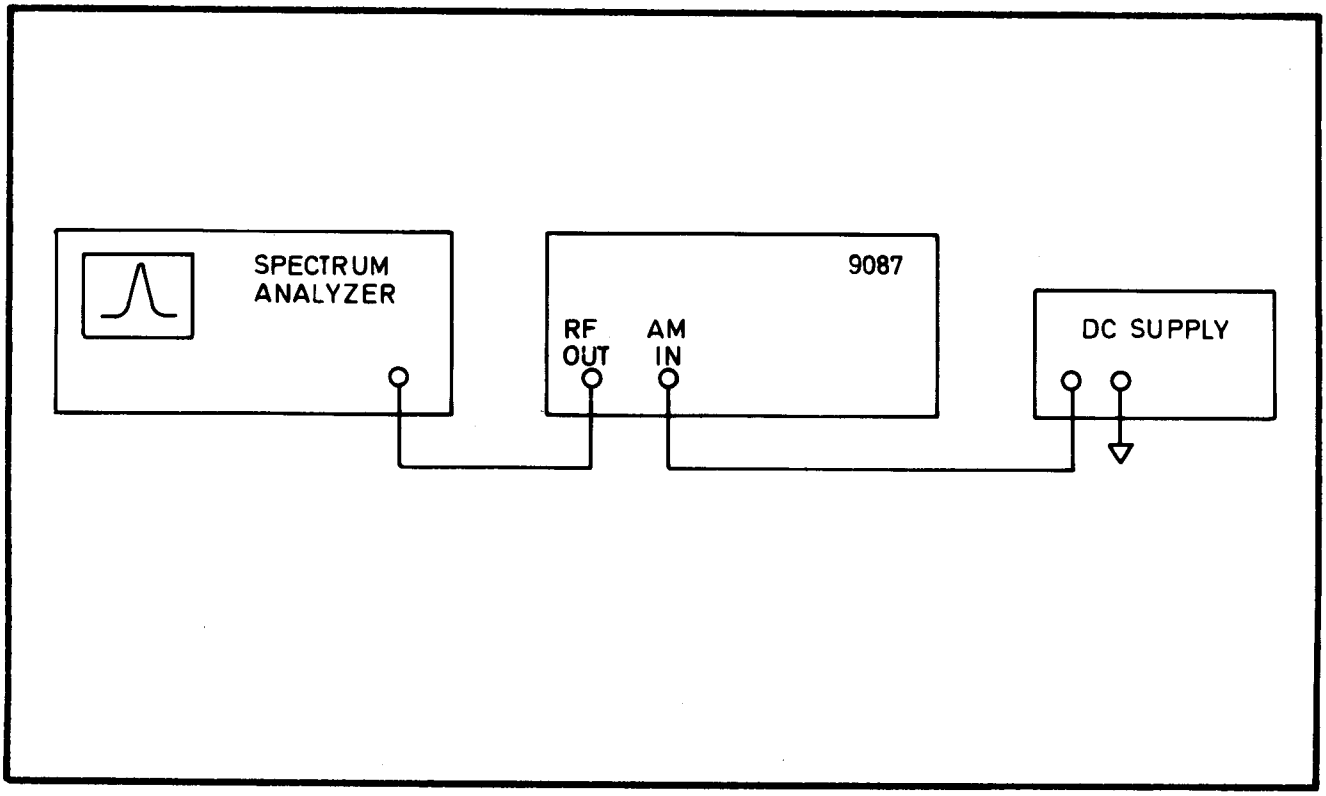


Fig. 7.24 Connections for Pulse Modulation PVP

7.9.2.5.9 Use the following series of steps to complete the pulse modulation verification:

(a) Initialize the 9087.

(b) Connect the power supply to the AM/PULSE input on the 9087.

(c) Select EXT DC PULSE ON and vary the input voltage to the 9087 from 0 to +2 V.

(d) Verify Table 7.32.

> NOTE
>
> After approximately 10 seconds in the "carrier off" condition, ERROR 88 should appear.

(e) Set the 9087 to 1300 MHz, +19 dBm, 400 Hz INT. pulse modulation.

(f) Tune in the spectrum analyzer and with the scan-width set to 0 Hz, determine the ON/OFF ratio and record it in Table 7.33.

(g) Repeat this test at 749 MHz.

7.9.2.6 SSB Phase Noise PVP (Optional)

7.9.2.6.1 Test equipment required:

Item	Table 7.1 Item No.
Spectrum Analyzer System	9

7.9.2.6.2 Measurement of the extremely low phase noise of the 9087 is difficult and complicated. The test equipment is specialized and requires detailed and in-depth knowledge of the measurement technique. It must be used in accordance with the manufacturer's instructions.

7.9.2.6.3 It is recommended that phase-noise measurements be conducted at the following carrier frequencies and at offsets from 100 Hz to 10 MHz for options 04A and 04B, and offsets from 1 Hz to 10 MHz for Option 04L5:

Carrier Frequencies Suggested: 1300 MHz
1000 MHz
700 MHz

> NOTE
>
> Phase noise tests are very time consuming and it is suggested that the user check the calibration at his own particular frequency of interest.

7.9.2.7 Broadband Noise Floor PVP (Optional)

7.9.2.7.1 Test equipment required:

Item	Table 7.1 Item No
Spectrum Analyzer System	9

7.9.2.7.2 Use the test equipment in accordance with the manufacturer's instructions to measure the broadband noise floor. The value should be not more than -150 dBc/Hz. Record the measured level in the box.

7.9.2.8 Spectral Purity PVP

7.9.2.8.1 Test equipment required:

Item	Table 7.1 Item No
Spectrum Analyzer	7

7.9.2.8.2 This PVP assesses the 9087's frequency response at frequencies where spurious and harmonic signals are most likely to be generated. Connect the test equipment as shown in Fig. 7.25.

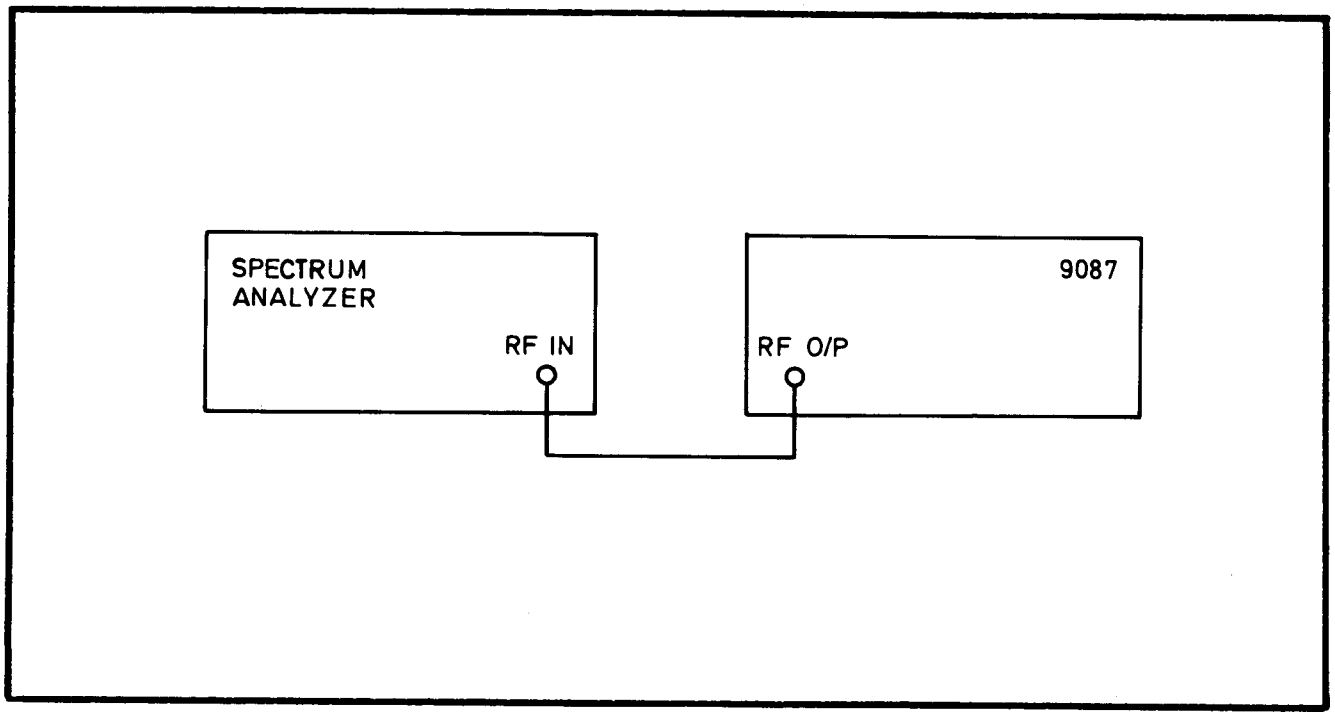


Fig. 7.25 Connections for Spectral Purity PVP

7.9.2.8.3 Use the following steps to complete the spurious frequency verification:

(a) Connect the spectrum analyzer to the RF output of the 9087 and initialize the 9087. The analyzer's step-width should be set to 2 MHz.

(b) Adjust the 9087 carrier frequency to 50 MHz and set the output amplitude to +13 dBm.

(c) Set the analyzer controls to give the minimum input attenuation allowable with +13 dBm input, 100 kHz resolution bandwidth, scan-width of 10 MHz/division, video filter OFF, and reference level of +13 dBm.

(d) Adjust the analyzer from 0 to 1.3 GHz. Check that any spurious frequencies are below -90 dBc. Enter the measured level of any spurious frequencies in Table 7.34.

(e) Repeat with the carrier frequency set to 753.123456 MHz. Check that any spurious frequencies are below -85 dBc. Enter the measured level of any spurious frequencies in Table 7.34.

NOTE

(1) If noise level is too high at any point, reduce the bandwidth or add video filtering. However, the sweep must be adjusted to maintain the amplitude calibrated.

(2) The input mixer of the spectrum analyzer is driven harder than its optimum level during this test in order to maximize sensitivity. This could lead to the generation of spurious signals within the spectrum analyzer. Therefore, any spurious signal observed must be verified as being produced by the 9087. This may be achieved by adding 10 dB of attenuation to the RF input of the spectrum analyzer. If the spurious signal level remains the same (i.e., relative to the carrier or reference signal), then it is probably being generated in the 9087. However, if its level falls or it disappears, then the spurious signal is due to the spectrum analyzer itself.

(3) This PVP for 9087 spectral purity can be limited to the user's particular band of interest if desired.

7.9.2.8.4 Use the following series of steps to complete the line-related spurious frequency verification:

(a) Set the 9087 to 1 GHz at a +13 dBm output level.

(b) Set the analyzer resolution bandwidth to 10 Hz and scan-width to 300 Hz.

(c) Check that all spurious signals at harmonics of the line frequency are lower than -64 dBc (i.e. 50, 100, 150 etc. Hz or 60, 120, 180 etc. Hz).

(d) Indicate the measured line-related spurious frequencies in Table 7.35.

7.9.2.8.5 Use the following series of steps to complete the harmonic frequency verification:

(a) Set the 9087 amplitude to +13 dBm.

(b) Set the 9087 frequency to the values shown in Table 7.36.

(c) Check that the second and third harmonics at each frequency are below the values shown and note these measurements in Table 7.36.

7.9.2.9 Internal Frequency Standard PVP

7.9.2.9.1 Test equipment required:

Item	Table 7.1 Item No
Oscilloscope	10
Frequency Standard	11
RF Level Meter	16

NOTE

Before checking and adjusting (if necessary) the internal reference oscillator, the 9087 should be permitted a warm-up period of at least one day for each month that the instrument has been left unpowered. This warm-up period should be a minimum of 24 hours. (The instrument may be left in standby mode during this warm-up period). The appropriate warm-up period for the external reference frequency standard must also be allowed.

7.9.2.9.2 Connect the test equipment as shown in Fig. 7.26.

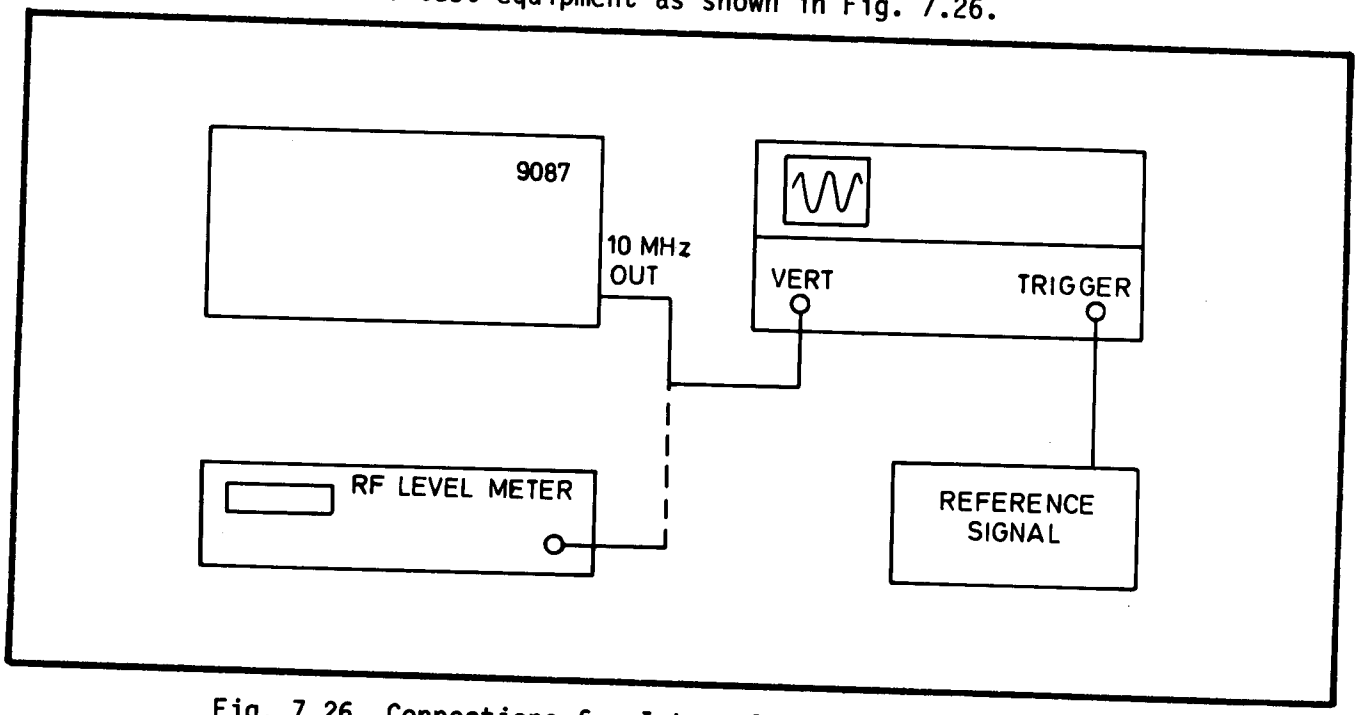


Fig. 7.26 Connections for Internal Frequency Standard PVP

7.9.2.9.3 Use the following series of steps to complete the internal standard verification:

(a) With the 10 MHz standard output from the 9087 connected to the vertical input of the oscilloscope and the reference signal to the external trigger input, adjust the internal oscillator for a stationary trace on the oscilloscope.

(b) Disconnect the 9087 10 MHz output from the oscilloscope and connect it to the input of the RF level meter. The output level should be 0 dBm ± 2 dB.

7.9.2.10 External Standard Input PVP

7.9.2.10.1 Test equipment required:

Item	Table 7.1 Item No
Signal Generator	12

7.9.2.10.2 Use the following series of steps to complete this verification:

(a) Connect the 10 MHz signal to the external standard input of the 9087, as shown in Fig. 7.27. Select EXT on the 9087 internal/external frequency standard selector.

(b) Check that ERROR 80 is not produced in the 9087 for the input signal frequencies shown in Table 7.37.

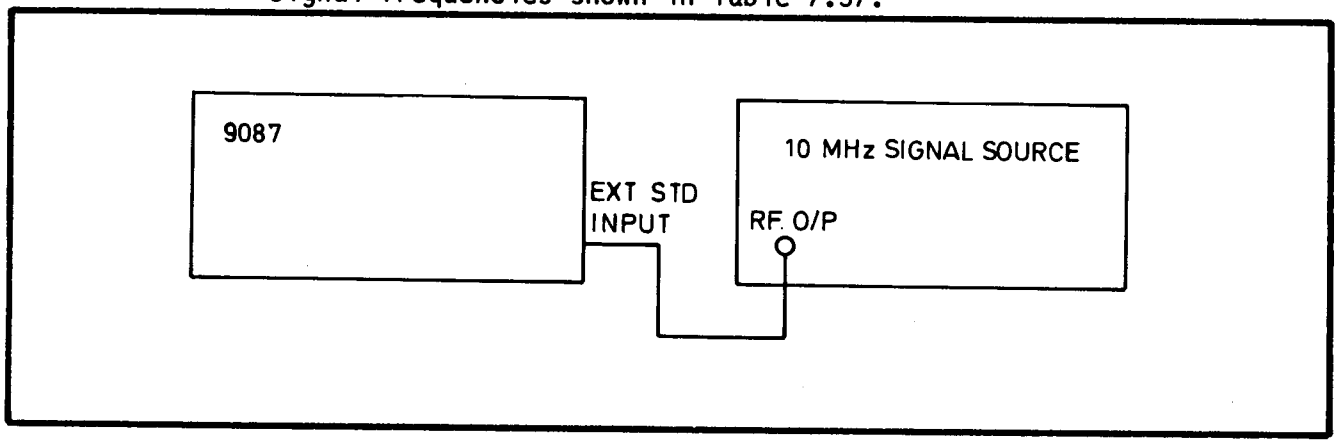


Fig. 7.27 Connections for External Frequency Standard PVP

7.9.3 ALTERNATIVE PVPs

7.9.3.1 Output Level Accuracy and Flatness PVP

7.9.3.1.1 Test equipment required:

Item	Table 7.1 Item No7
Wattmeter	4

7.9.3.1.2 The verification procedure to be used is given in paragraph 7.9.2.2. The wattmeter is connected in place of the measuring receiver.

7.9.3.2 Attenuator PVP

7.9.3.2.1 Test equipment required:

Item	Table 7.1 Item No
Spectrum Analyzer	14
Calibrated Attenuator Pads	15

7.9.3.2.2 Use the following series of steps to complete the attenuator verification:

(a) Initialize the 9087.

(b) Set the amplitude to +12.9 dBm.

(c) Connect the 9087 to the spectrum analyzer.

(d) Center the analyzer trace on the carrier, then set the reference level to the carrier peak.

(e) Connect the 9087 using the 10 dB attenuator pad. Set the analyzer marker and delta (Δ) marker to the carrier peak.

(f) Remove the attenuator pad and reconnect the 9087.

(g) Set the amplitude to +2.9 dBm.

(h) The attenuation of the 9087 attenuator is then given by the pad attenuation plus the delta marker reading.

(j) Repeat the entire above-described procedure, substituting in the procedure either the 20, 40, or 80 dB pad and setting the amplitude to the levels indicated in Table 7.38.

7.9.3.3 Audio Output PVP

7.9.3.3.1 Test equipment required:

Item	Table 7.1 Item No
Frequency Counter	2
Frequency Distribution System	13
True RMS Voltmeter	16
Distortion Analyzer	17

7.9.3.3.2 Use the following series of steps to complete the procedure for frequency verification:

(a) Connect the 400 Hz output from the 9087 to the Channel A input on the counter, with the counter set to measure frequency A with 0.1 Hz resolution.

(b) Connect the 10 MHz standard output from the 9087 to the external standard input on the frequency meter via the frequency distribution system. Set the frequency meter selector to EXTERNAL.

(c) Record the frequency in Table 7.39.

(d) Connect the 1 kHz output from the 9087 (as described in step (a)) and measure/record the frequency.

7.9.3.3.3 Use the following series of steps to complete the procedure for output voltage level verification:

(a) Connect the test equipment as shown in Fig. 7.28.

(b) Measure the voltage output at both the 400 Hz and 1 kHz audio outputs.

(c) Record the measured values in Table 7.40.

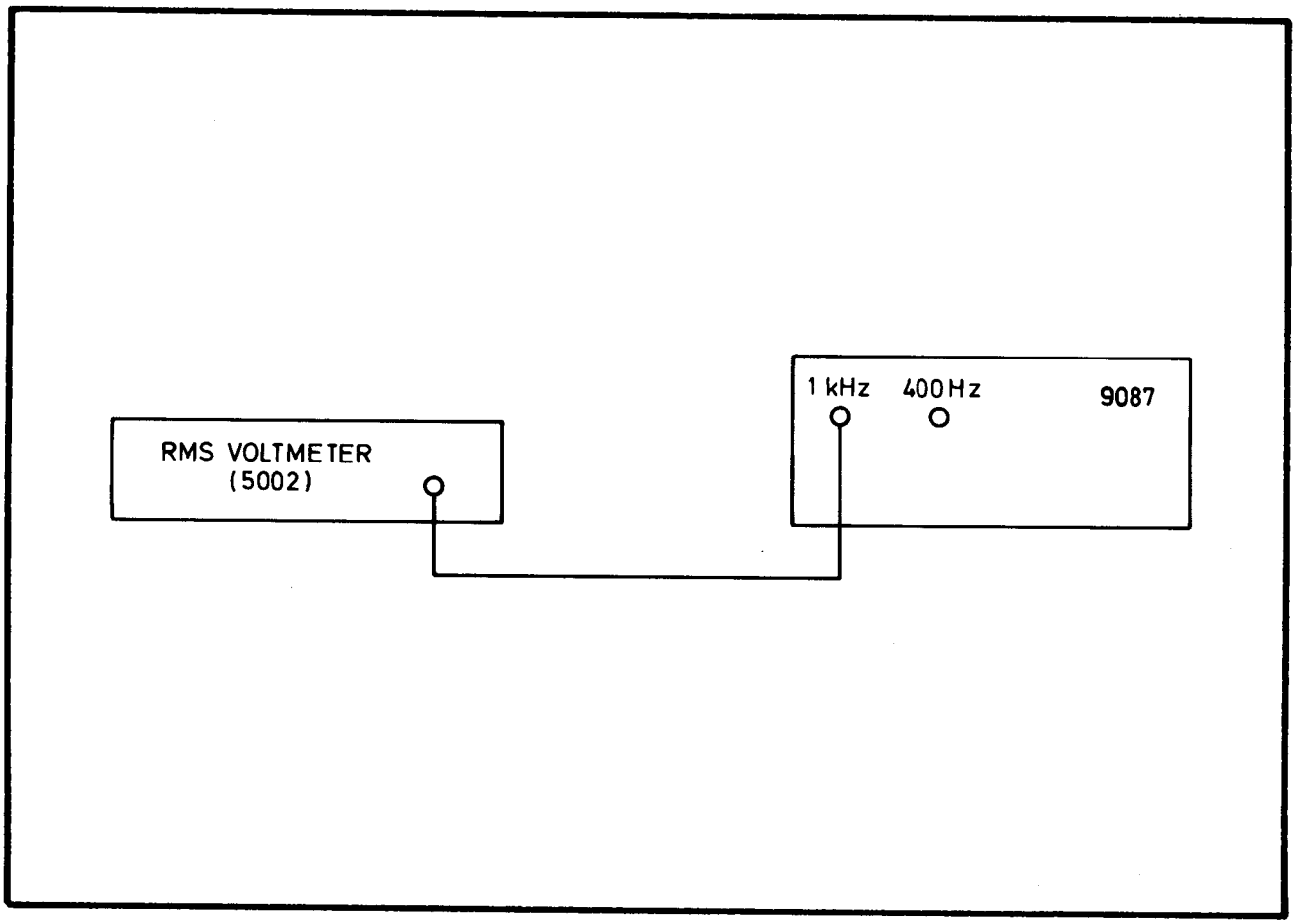


Fig. 7.28 Connections for Output Level Verification

NOTE

The output voltage limits indicated in Table 7.40 include the accuracy of the 5002 digital multimeter.

7.9.3.3.4 Use the following series of steps to complete the distortion level verification procedure:

(a) Connect the test equipment as shown in Fig. 7.29.

(b) Measure the total harmonic distortion from the 400 Hz and 1 kHz audio outputs of the 9087.

(c) Record the measured values in Table 7.41.

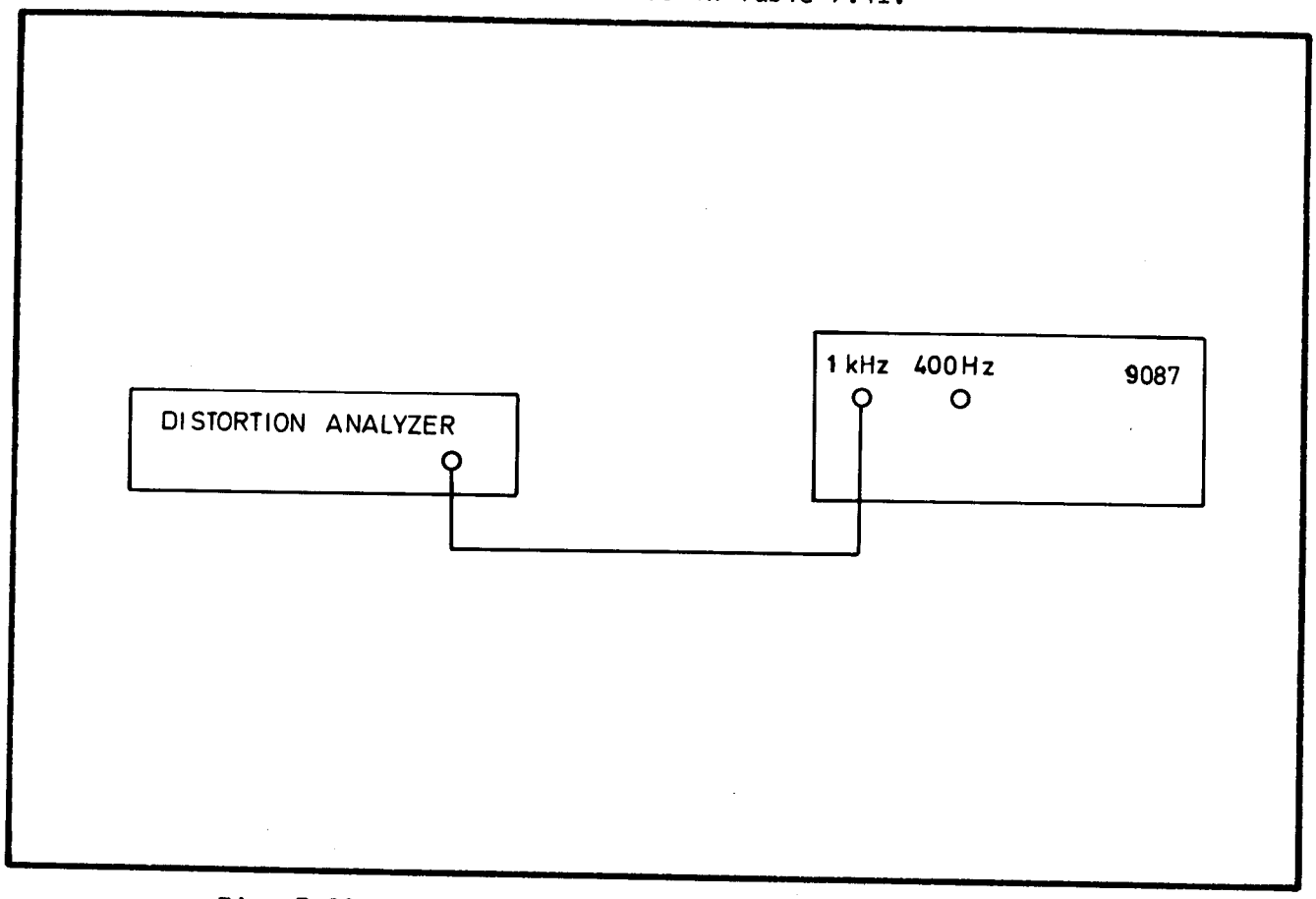


Fig. 7.29 Connections for Distortion Level Verification

7.9.3.4 Internal Frequency Modulation PVP

7.9.3.4.1 Test equipment required:

Item	Table 7.1 Item No
Modulation Analyzer	18
Distortion Analyzer	17

7.9.3.4.2 Connect the test equipment as shown in Fig. 7.30. Carry out the internal frequency modulation verification in accordance with the instructions given in paragraph 7.9.2.5.3.

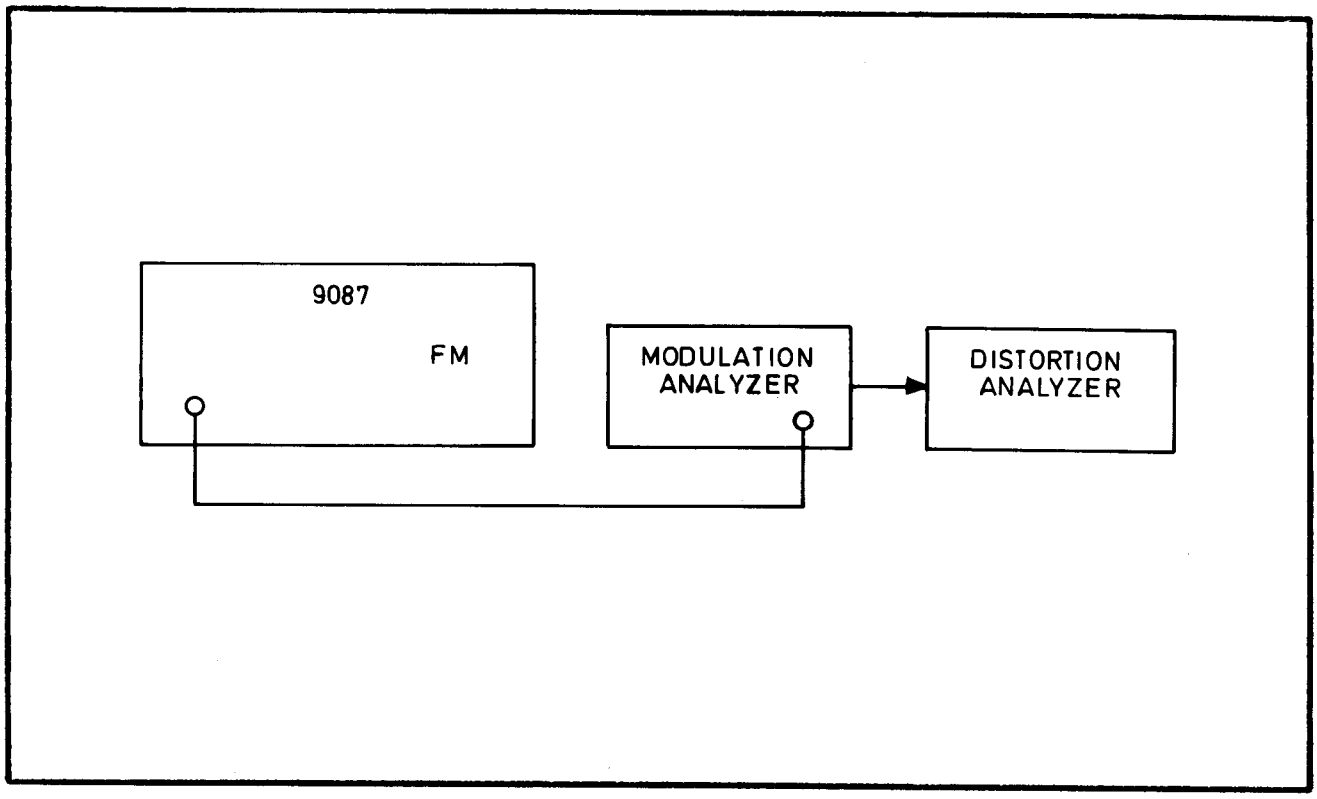


Fig. 7.30 Connections for Internal Frequency Modulation Verification

7.9.3.5 Broadband Noise Floor PVP (Optional)

7.9.3.5.1 Test equipment required:

Item	Table 7.1 Item No
Spectrum Analyzer	14
Coaxial Notch Filter	19
T piece	20

7.9.3.5.2 The noise floor level is determined by means of the following measured parameters:

(a) Analyzer noise measurement in dBm (A)

(b) Carrier level in dBm (C)

(c) Reference level of +13 dBm (R)

7.9.3.5.3 Use the following series of steps to measure the parameters and calculate the broadband noise floor:

(a) Initialize the 9087.

(b) Set the frequency to 500 MHz and connect the 9087 directly to the spectrum analyzer without the coaxial stub attached.

(c) Set the 9087 amplitude to +13 dBm (R).

(d) Set the analyzer reference level to the carrier peak.

(e) Connect the coaxial stub at the 9087 end of the connection to the analyzer, as shown in Fig. 7.31.

(f) Adjust the 9087 output frequency to the notch frequency, at which the carrier level observed on the spectrum analyzer is a minimum.

(g) Set the analyzer frequency to 200 MHz above the notch frequency.

(h) Set the analyzer attenuation to 0 dB.

(j) Reduce the scan-width of the analyzer to 1 MHz. The resolution bandwidth should be 10 kHz.

(k) Switch the 9087 output OFF and observe the drop in the analyzer noise level.

(l) Note the noise level with the output ON (A).

(m) Increase the 9087 frequency by 200 MHz and note the carrier level (C).

(n) Calculate the broadband noise level from the expression:

A-(R-C)-10 $\log_{10}$ (resolution bandwidth of the analyzer) - 2.5 dB.

Where R-C is the stub loss, and the 2.5 dB term is the video averaging correction factor.

(p) Ensure that the broadband noise level is not more than -150 dBc/Hz and indicate the value in the box.

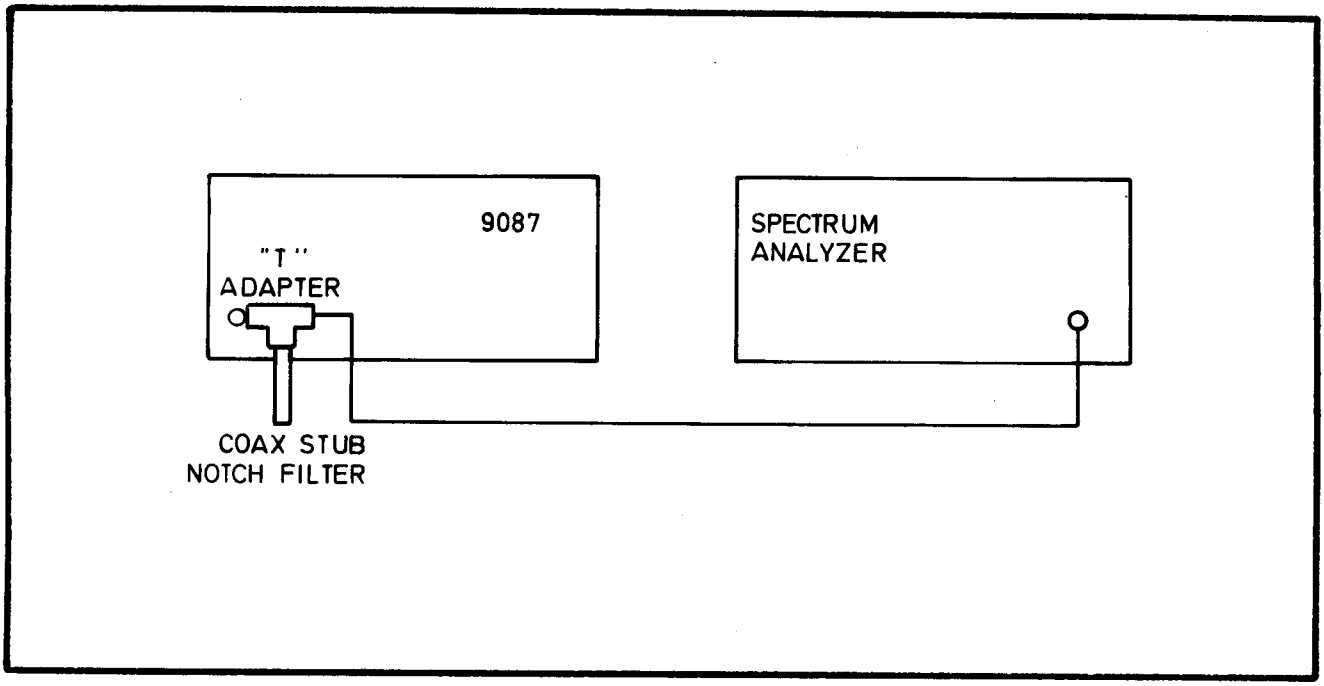


Fig. 7.31 Connections for Broadband Noise Floor Verification

TABLE 7.19

Frequency Verification

Set Frequency	Measured Frequency Tolerance ± 1 Hz
10.000 000 MHz	
101.111 111 MHz	
104.000 000 MHz	
107.000 000 MHz	
109.000 000 MHz	
112.000 000 MHz	
114.000 000 MHz	
117.000 000 MHz	
122.000 000 MHz	
147.000 000 MHz	
225.000 000 MHz	
308.641 973 MHz	
411.111 111 MHz	
555.277 778 MHz	
641.500 000 MHz	
711.111 111 MHz	
1000.000 000 MHz	

TABLE 7.20

Output Level Accuracy Measurements

Frequency	Minimum Limit	Measured Value	Maximum Limit
Output Level set to + 3 dBm			
1 MHz	+ 2.4 dBm		+ 3.6 dBm
2 MHz	+ 2.4 dBm		+ 3.6 dBm
5 MHz	+ 2.4 dBm		+ 3.6 dBm
10 MHz	+ 2.4 dBm		+ 3.6 dBm
20 MHz	+ 2.4 dBm		+ 3.6 dBm
50 MHz	+ 2.4 dBm		+ 3.6 dBm
100 MHz	+ 2.4 dBm		+ 3.6 dBm
200 MHz	+ 2.4 dBm		+ 3.6 dBm
500 MHz	+ 2.4 dBm		+ 3.6 dBm
750 MHz	+ 2.0 dBm		+ 4.0 dBm
1000 MHz	+ 2.0 dBm		+ 4.0 dBm
1300 MHz	+ 2.0 dBm		+ 4.0 dBm
Output Level set to + 9 dBm			
1 MHz	+ 8.4 dBm		+ 9.6 dBm
2 MHz	+ 8.4 dBm		+ 9.6 dBm
5 MHz	+ 8.4 dBm		+ 9.6 dBm
10 MHz	+ 8.4 dBm		+ 9.6 dBm
20 MHz	+ 8.4 dBm		+ 9.6 dBm
50 MHz	+ 8.4 dBm		+ 9.6 dBm
100 MHz	+ 8.4 dBm		+ 9.6 dBm
200 MHz	+ 8.4 dBm		+ 9.6 dBm
500 MHz	+ 8.4 dBm		+ 9.6 dBm
750 MHz	+ 8.0 dBm		+ 10.0 dBm
1000 MHz	+ 8.0 dBm		+ 10.0 dBm
1300 MHz	+ 8.0 dBm		+ 10.0 dBm

TABLE 7.20 (Continued)

Output Level Accuracy Measurements

Frequency	Minimum Limit	Measured Value	Maximum Limit
Output Level set to + 13 dBm			
1 MHz	+ 12.4 dBm		+ 13.6 dBm
2 MHz	+ 12.4 dBm		+ 13.6 dBm
5 MHz	+ 12.4 dBm		+ 13.6 dBm
10 MHz	+ 12.4 dBm		+ 13.6 dBm
20 MHz	+ 12.4 dBm		+ 13.6 dBm
50 MHz	+ 12.4 dBm		+ 13.6 dBm
100 MHz	+ 12.4 dBm		+ 13.6 dBm
200 MHz	+ 12.4 dBm		+ 13.6 dBm
400 MHz	+ 12.4 dBm		+ 13.6 dBm
500 MHz	+ 12.4 dBm		+ 13.6 dBm
750 MHz	+ 12.0 dBm		+ 14.0 dBm
1000 MHz	+ 12.0 dBm		+ 14.0 dBm
1300 MHz	+ 12.0 dBm		+ 14.0 dBm
Output Level set to + 19 dBm			
1 MHz	+ 18.1 dBm		+ 19.9 dBm
2 MHz	+ 18.1 dBm		+ 19.9 dBm
5 MHz	+ 18.1 dBm		+ 19.9 dBm
10 MHz	+ 18.1 dBm		+ 19.9 dBm
20 MHz	+ 18.1 dBm		+ 19.9 dBm
50 MHz	+ 18.1 dBm		+ 19.9 dBm
100 MHz	+ 18.1 dBm		+ 19.9 dBm
200 MHz	+ 18.1 dBm		+ 19.9 dBm
500 MHz	+ 18.1 dBm		+ 19.9 dBm
750 MHz	+ 17.9 dBm		+ 20.1 dBm
1000 MHz	+ 17.9 dBm		+ 20.1 dBm
1300 MHz	+ 17.9 dBm		+ 20.1 dBm

Output Level Flatness

BELOW 650 MHz	

ABOVE 650 MHz	

TABLE 7.21

Attenuator Verification

Amplitude Setting for 9087	Attenuation		
	Minimum Limit	Measured dB	Maximum Limit
+12.9 dBm	---	Reference Level	---
+2.9 dBm	9.9 dB		10.1 dB
-7.1 dBm	19.8 dB		20.2 dB
-27.1 dBm	39.6 dB		40.4 dB
-67.1 dBm	79.2 dB		80.8 dB

TABLE 7.22

Audio Frequency Measurement

Frequency	Minimum Limit	Measured Frequency	Maximum Limit
400 Hz	399.9 Hz		400.1 Hz
1 kHz	999.9 Hz		1000.1 Hz

TABLE 7.23

Audio Output Level and Distortion

Frequency	Output Level			Distortion	
	Minimum Limit	Measured Value	Maximum Limit	Measured Value	Maximum Limit
400 Hz	1.88 V		2.13 V		1%
1 kHz	1.88 V		2.13 V		1%

TABLE 7.24

Internal Frequency Modulation Verification

Carrier Frequency	Modulation Frequency	Deviation Setting	Deviation			Distortion	
			Minimum Limit	Measured Value	Maximum Limit	Measured Value	Maximum Limit
1000 MHz	1 kHz	30 kHz	28.5 kHz		31.5 kHz		1%
325 MHz	1 kHz	300 kHz	285.0 kHz		315.0 kHz		1%
324 MHz	1 kHz	300 kHz	285.0 kHz		315.0 kHz		3%
50 MHz	1 kHz	10 kHz	9.0 kHz		11.0 kHz		1%

TABLE 7.25

High/Low Limit Detector Check

Voltage Input (r.m.s.)	With FM/AM EXT AC Selected		
	LED	Checks	
		FM	AM
0.18 V	Low On		
0.21 V to 1.98 V	Both Off		
2.2 V	High On		

TABLE 7.26

External Frequency Modulation Verification

Carrier Frequency	Modulation Frequency	Deviation Setting	Minimum Limit	Measured Deviation	Maximum Limit
324 MHz	1 kHz	300 kHz	285 kHz		315 kHz
324 MHz	100 kHz	50 kHz	35 kHz		65 kHz

External DCFM Frequency Offset

TABLE 7.27

Phase Modulation at 1 kHz Internal Modulation

Modulation Frequency	Peak Phase Modulation	Deviation			Distortion	
		Minimum Limit	Measured Value	Maximum Limit	Measured Value	Measured Limit
1 kHz Int.	5.0 rads	4.5 rads		5.5 rads		3%

TABLE 7.28

Phase Modulation at 10 kHz External Modulation

Modulation Frequency	Peak Phase Deviation	Deviation		
		Minimum Limit	Measured Value	Maximum Value
10 kHz	5.0	3.5 rads		6.5 rads

TABLE 7.29

Amplitude Modulation at 80% with 1 kHz INT Modulation

Carrier Frequency	Modulation Depth			Distortion	
	Minimum Limit	Measured Value	Maximum Limit	Measured Value	Maximum Limit
1.5 MHz	75.4%		84.6%		3%
5 MHz	75.4%		84.6%		3%
10 MHz	75.4%		84.6%		3%
50 MHz	75.4%		84.6%		3%
100 MHz	75.4%		84.6%		3%
500 MHz	75.4%		84.6%		3%
600 MHz	75.4%		84.6%		3%
1000 MHz	75.4%		84.6%		3%
1300 MHz	75.4%		84.6%		3%

TABLE 7.30

Amplitude Modulation at 30% with 1 kHz INT Modulation

Carrier Frequency	Modulation Depth			Distortion	
	Minimum Limit	Measured Value	Maximum Limit	Measured Value	Maximum Limit
1.5 MHz	26.4%		33.6%		1.5%
5 MHz	26.4%		33.6%		1.5%
10 MHz	26.4%		33.6%		1.5%
50 MHz	26.4%		33.6%		1.5%
100 MHz	26.4%		33.6%		1.5%
500 MHz	26.4%		33.6%		1.5%
600 MHz	26.4%		33.6%		1.5%
1000 MHz	26.4%		33.6%		1.5%
1300 MHz	26.4%		33.6%		1.5%

TABLE 7.31

External Amplitude Modulation at 80%

Carrier Frequency	Modulating Frequency	Modulation Depth		
		Low Limit	Measured Value	High Limit
1300 MHz	1 kHz	75.4%		84.6%
1300 MHz	20 kHz	56%		84.6%

TABLE 7.32

Preliminary Pulse Modulation Verification

Input Voltage	Carrier On/Off	Check
<0.9 V	Off	
>1.7 V	On	

TABLE 7.33

Pulse Modulation Measurements

Frequency	Carrier On/Off Ratio	
	Minimum Limit	Measured Value
1300 MHz 749 MHz	35 dB 50 dB	

Broadband Noise Floor

TABLE 7.34

Spurious Signal Measurement

Carrer Frequency	Spurious Signal Level	
	Maximum Limit	Measured Value
50 MHz 753.123456 MHz	-90 dBc -85 dBc	

TABLE 7.35

Line-Related Spurious Signal Measurement

	Line Related Spurious Signals	
	Measured Level	Maximum Level
Line-Related Sidebands		-64 dBc

TABLE 7.36

Harmonic Frequency Measurement

Carrier Frequency	Measured Harmonic Signal Level			
	2nd	3rd	Others	Maximum Limit
0.1 MHz				-33 dBc
0.15 MHz				-33 dBc
0.4 MHz				-33 dBc
1.5 MHz				-33 dBc
15.0 MHz				-33 dBc
30.0 MHz				-33 dBc
99.0 MHz				-33 dBc
100.0 MHz				-33 dBc
129.0 MHz				-33 dBc
130.0 MHz				-33 dBc
159.0 MHz				-33 dBc
160.0 MHz				-33 dBc
229.0 MHz				-33 dBc
230.0 MHz				-33 dBc
324.0 MHz				-33 dBc
325.0 MHz				-33 dBc
459.0 MHz				-33 dBc
460.0 MHz				-33 dBc
649.0 MHz				-33 dBc
650.0 MHz				-27 dBc
750.0 MHz				-27 dBc
919.0 MHz				-27 dBc
920.0 MHz				-27 dBc
1100.0 MHz				-27 dBc
1300.0 MHz				-27 dBc

TABLE 7.37

External Standard Input Signal Locking

Input Signal Frequency in Hz	External Standard Input Level	External Standard Input Signal Locking
9 999 900 Hz	1.0 V	
10 000 100 Hz	1.0 V	

TABLE 7.38

Attenuator Verification

Amplitude Setting for 9087	Attenuation		
	Minimum Limit	Measured Value	Maximum Limit
+12.9 dBm		Reference Level	
+2.9 dBm (Use 10 dB pad)	9.9 dB		10.1 dB
-7.1 dBm (Use 20 dB pad)	19.8 dB		20.2 dB
-27.1 dBm (Use 40 dB pad)	39.6 dB		40.4 dB
-67.1 dBm (Use 80 dB pad)	79.2 dB		80.8 dB

TABLE 7.39

Frequency Measurement for Audio Output Verification

Frequency	Minimum Limit	Measured Value	Maximum Limit
400 Hz 1 kHz	399.9 Hz 999.9 Hz		400.1 Hz 1000.1 Hz

TABLE 7.40

Audio Output Level

Frequency	Minimum Limit	Measured Value	Maximum Limit
400 Hz 1 kHz	1.88 V 1.88 V		2.13 V 2.13 V

TABLE 7.41

Audio Output Distortion

Frequency	Distortion	
	Measured Value	Maximum Limit
400 Hz		1.0%
1 kHz		1.0%

Broadband Noise Level

SECTION 8

PARTS LIST AND CIRCUIT DIAGRAMS

PARTS LIST

CHASSIS ASSEMBLY 11-1520

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Cable Assemblies					
RCØ		Coaxial cable assembly			10-2775
RC1		Coaxial cable assembly			10-2832
RCØ		Coaxial cable assembly (rear panel option)			10-2875
RC1		Coaxial cable assembly (rear panel option)			10-2876
PL11-PL25		Ribbon cable assembly			10-2826
PL10-PL24		Ribbon cable assembly			10-2827
Power Switch					
S1		Switch, DPST, with flexible connector			23-4117
		Knob for 23-4117			23-9098
Sub Assembly					
		Attenuator assembly			11-1526

Note: When ordering a replacement attenuator it is essential that the list of option codes shown on the rear panel is quoted in addition to the part number.

PARTS LIST

FRONT AND REAR PANEL ASSEMBLIES

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
FRONT PANEL ASSEMBLY 11-1529					
Cable Assemblies					
FC4		Coaxial cable assembly			10-2784
FC5		Coaxial cable assembly			10-2785
FC4		Coaxial cable assembly (rear panel option)			10-2877
FC5		Coaxial cable assembly (rear panel option)			10-2878
Spinwheel					
		Spinwheel assembly			11-1588
		Knob for spinwheel			15-0573
Miscellaneous					
SK2		BNC bulkhead receptacle			23-3005
SK3		BNC bulkhead receptacle			23-3005
		Touch panel			13-1846
		Clunker			23-9111
REAR PANEL ASSEMBLY 11-1530					
Cable Assemblies					
FC9		Coaxial cable assembly			10-2795
FC7		Coaxial cable assembly			10-2796
FC6		Coaxial cable assembly			10-2797
FC8		Coaxial cable assembly			10-2798
PL9-SK70		Ribbon cable assembly			10-2830
Connectors					
SK72		BNC, bulkhead receptacle			23-3005
SK73		BNC, bulkhead receptacle			23-3005
SK74		BNC, bulkhead receptacle			23-3005
SK75		BNC, bulkhead receptacle			23-3005
SK76		BNC, bulkhead receptacle			23-3005
SK77		BNC, bulkhead receptacle			23-3005

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Sub Assemblies					
		Fan			17-1033
		Frequency standard (Racal-Dana)			9442/5
		Frequency standard (Austron)			23-9127

PARTS LIST

DISPLAY ASSEMBLY 19-1041

Fig 4

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors					
	Ω		W		
R1	1k	Carbon Film	¼	5	20-2102
R2	270	Carbon Film	¼	5	20-2271
R3	270	Carbon Film	¼	5	20-2271
R4	330	Carbon Film	¼	5	20-2331
R5	1k	Carbon Film	¼	5	20-2102
R6	10k	Carbon Film	¼	5	20-2103
R7	10k	Carbon Film	¼	5	20-2103
R8	10k	Carbon Film	¼	5	20-2103
R9	330	Carbon Film	¼	5	20-2331
R10	1k	Carbon Film	¼	5	20-2102
R11	100	Carbon Film	¼	5	20-2101
R12	680	Carbon Film	¼	5	20-2681
R13	47k	Carbon Film	¼	5	20-2473
R14	47k	Carbon Film	¼	5	20-2473
R15	680	Carbon Film	¼	5	20-2681
R16	220k	Carbon Film	¼	5	20-2224
R17	220k	Carbon Film	¼	5	20-2224
R18	270	Carbon Film	¼	5	20-2271
R19	270	Carbon Film	¼	5	20-2271
R20	10M	Carbon Film	¼	5	20-2106
R21	2.2M	Carbon Film	¼	5	20-2225
R22		Not Used			
R23	180	Carbon Film	¼	5	20-2181
R24	1k	Carbon Film	¼	5	20-2102
R25	5 x 220	DIL Array			20-5529
R26	5 x 220	DIL Array			20-5529
R27	5 x 220	DIL Array			20-5529
R28	9 x 220	DIL Array			20-5530
R29	5 x 220	DIL Array			20-5529
R30	9 x 220	DIL Array			20-5530
R31	9 x 220	DIL Array			20-5530
R32	5 x 220	DIL Array			20-5529
R33	9 x 220	DIL Array			20-5530
R34	220	Carbon Film	¼	5	20-2221
R35	5 x 220	DIL Array			20-5529

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R36	5 x 220	DIL Array			20-5529
R37	5 x 220	DIL Array			20-5529
R38	5 x 220	DIL Array			20-5529
R39	9 x 220	DIL Array			20-5530
R40	9 x 220	DIL Array			20-5530
R41	9 x 220	DIL Array			20-5530
R42	9 x 220	DIL Array			20-5530
R43		Not Used			
R44	1k	Carbon Film	¼	5	20-2102
Capacitors					
	F		V		
C1	47µ	Electrolytic	6.3		21.0704
C2	100n	Ceramic	12	-20+80	21-1616
C3	47µ	Electrolytic	6.3		21-0704
C4	100n	Ceramic	12	-20+80	21-1616
C5	47µ	Electrolytic	6.3		21-0704
C6	100n	Ceramic	12	-20+80	21-1616
C7	47µ	Electrolytic	6.3		21-0704
C8	100n	Ceramic	12	-20+80	21-1616
C9	100n	Ceramic	12	-20+80	21-1616
C10	100n	Ceramic	12	-20+80	21-1616
C11	100n	Ceramic	12	-20+80	21-1616
C12	100n	Ceramic	12	-20+80	21-1616
C13	100n	Ceramic	12	-20+80	21-1616
C14	100n	Ceramic	12	-20+80	21-1616
C15	100n	Ceramic	12	-20+80	21-1616
C16	100n	Ceramic	12	-20+80	21-1616
C17	100n	Ceramic	12	-20+80	21-1616
C18	100n	Ceramic	12	-20+80	21-1616
C19	100n	Ceramic	12	-20+80	21-1616
C20	100n	Ceramic	12	-20+80	21-1616
C21	100n	Ceramic	12	-20+80	21-1616
C22	220p	Ceramic	500	10	21-1524
Diodes					
D1		1N4149			22-1029
D2		1N4149			22-1029
D3		1N4149			22-1029

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
LP1		LED, red (HLMP-2300)			26-5016
LP2		LED, red (HLMP-2300)			26-5016
LP3		LED, red (HLMP-2350)			26-5017
LP4		LED, red (MV57641)			26-5025
LP5		LED, red (HLMP-2300)			26-5016
LP6		LED, red (HLMP-2300)			26-5016
LP7		LED, red (HLMP-2300)			26-5016
LP8		LED, red (HLMP-2300)			26-5016
LP9		LED, red (HLMP-2300)			26-5016
LP10		LED, red (HLMP-2300)			26-5016
LP11		LED, red (HLMP-2300)			26-5016
LP12		LED, red (HLMP-2300)			26-5016
LP13		LED, red (HLMP-2300)			26-5016
LP14		LED, red (HLMP-2300)			26-5016
LP15		LED, red (HLMP-2300)			26-5016
LP16		LED, red (HLMP-2350)			26-5017
LP17		LED, red (HLMP-2350)			26-5017
LP18		LED, red (HLMP-2300)			26-5016
LP19		LED, red (HLMP-2300)			26-5016
LP20		Not Used			
LP21		LED, red (HLMP-2300)			26-5016
LP22		Not Used			
LP23		LED, red (HLMP-2350)			26-5017
LP24		Not Used			
LP25		Not Used			
LP26		Not Used			
LP27		Not Used			
LP28		Not Used			
LP29		Not Used			
LP30		Not Used			
LP31		LED, red (HLMP-2350)			26-5017
LP32		LED, red (HLMP-2350)			26-5017
LP33		LED, red (HLMP-2350)			26-5017
LP34		LED, red (HLMP-2300)			26-5016
LP35		LED, red (MV57124)			26-5018
LP36		LED, red (MV57124)			26-5018
LP37		LED, red (MV57124)			26-5018
LP38		LED, red (MV57124)			26-5018
LP39		LED, red (MV57124)			26-5018
LP40		LED, red (MV57124)			26-5018

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
LP41		LED, red (MV57124)			26-5018
LP42		LED, red (MV57124)			26-5018
LP43		LED, red (MV57124)			26-5018
LP44		LED, red (MV57124)			26-5018
LP45		LED, red (MV57124)			26-5018
LP46		LED, red (MV57124)			26-5018
LP47		LED, red (MV57124)			26-5018
LP48		LED, red (MV57124)			26-5018
LP49		LED, red (MV57124)			26-5018
LP50		LED, red (MV57124)			26-5018
LP51		LED, red (MV57124)			26-5018
LP52		LED, red (MV57124)			26-5018
LP53		LED, red (MV57124)			26-5018
LP54		LED, red (MV57124)			26-5018
LP55		LED, red (MV57124)			26-5018
LP56		LED, red (MV57124)			26-5018
LP57		LED, red (MV57124)			26-5018
LP58		LED, red (MV57124)			26-5018
LP59		LED, red (MV57124)			26-5018
LP60		LED, red (MV57124)			26-5018
LP61		LED, red (MV57124)			26-5018
LP62		LED, red (HLMP-2300)			26-5016
LP63		LED, red (HLMP-2300)			26-5016
LP64		LED, red (MV57124)			26-5018
LP65		LED, red (MV57124)			26-5018
LP66		LED, red (MV57124)			26-5018
LP67		LED, red (MV57124)			26-5018
LP68		LED, red (HLMP-2300)			26-5016
LP69		LED, red (HLMP-2300)			26-5016
LP70		LED, red (MV57124)			26-5018
LP71		LED, red (MV57124)			26-5018
LP72		LED, red (MV57124)			26-5018
LP73		LED, red (MV57124)			26-5018
LP74		LED, red (MV57124)			26-5018
LP75		LED, red (MV57124)			26-5018
Integrated Circuits					
IC1		74LS374			22-4672
IC2		74LS374			22-4672
IC3		74LS125			22-4657
IC4		74LS154			22-4589
IC5		TL082			22-4240

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
IC6		74LS379			22-4660
IC7		74LS00			22-4531
IC8		74LS374			22-4672
IC9		74LS367			22-4592
IC10		74LS244			22-4583
IC11		74LS138			22-4587
IC12		74LS374			22-4672
IC13		74LS75			22-4563
IC14		74LS37			22-4671
IC15		74LS75			22-4563
IC16		74LS156			22-4676
IC17		74LS154			22-4589
IC18		74LS377			22-4658
IC19		74LS02			22-4532
IC20		74LS04			22-4533
IC21		74LS379			20-4660
IC22		74LS378			22-4659
IC23		4093			22-4750
IC24		74LS51			22-4555
IC25		74LS51			22-4555
IC26		74LS378			22-4659
IC27		74LS378			22-4659
IC28		74LS379			22-4660
IC29		74LS374			22-4672
IC30		74LS378			22-4659
Transistors					
Q1		OPB706A			22-7102
Q2		OPB706A			22-7102
Numerical Indicators					
DI1		HDSP 0763			26-5021
DI2		HDSP 0761			26-5020
DI3		HDSP 0761			26-5020
DI4		HDSP 0761			26-5020
DI5		HDSP 0761			26-5020

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
DI6		HDSP 0761			26-5020
DI7		HDSP 0761			26-5020
DI8		HDSP 0761			26-5020
DI9		HDSP 0761			26-5020
DI10		HDSP 0761			26-5020
DI11		HDSP 0761			26-5020
DI12		HDSP 0761			26-5020
DI13		HDSP 0761			26-5020
DI14		HDSP 0761			26-5020
DI15		HDSP 0763			26-5021
DI16		HDSP 0761			26-5020
DI17		HDSP 0761			26-5020
DI18		HDSP 0761			26-5020
DI19		HDSP 0761			26-5020
DI20		HDSP 0761			26-5020
Connectors					
SK7		Cable Assembly			10-2695

PARTS LIST

MOTHERBOARD ASSEMBLY 19-1043

Fig 6

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors					
	Ω		W		
R1	1.5k	Carbon Film	¼	5	20-2152
R2	1.5k	Carbon Film	¼	5	20-2152
R3	10k	Metal Oxide	¼	2	20-4018
R4	1k	Carbon Film	¼	5	20-2102
R5	1k	Carbon Film	¼	5	20-2102
R6	10k	Metal Oxide	¼	2	20-4018
R7	3.3k	Carbon Film	0.1	5	20-1537
R8	5.6k	Carbon Film	0.1	5	20-1533
R9	10k	Carbon Film	¼	5	20-2103
R10	10k	Carbon Film	¼	5	20-2103
R11	3.3k	Carbon Film	¼	5	20-2332
R12	3.3k	Carbon Film	¼	5	20-2332
R13	47k	Carbon Film	0.1	5	20-1572
R14	10k	Carbon Film	0.1	5	20-1538
R15	10k	Carbon Film	0.1	5	20-1538
R16	1k	Carbon Film	¼	5	20-2102
R17	2.2k	Carbon Film	¼	5	20-2222
R18	10k	Carbon Film	¼	5	20-2103
R19	10k	Carbon Film	¼	5	20-2103
R20	68k	Carbon Film	¼	5	20-2683
R21	100k	Variable			20-7068
R22	4.7k	Carbon Film	¼	5	20-2472
R23	12k	Carbon Film	¼	5	20-2123
R24	12k	Carbon Film	¼	5	20-2123
R25	1k	Carbon Film	¼	5	20-2102
R26	1k	Carbon Film	¼	5	20-2102
R27	10k	Carbon Film	¼	5	20-2103
R28	3.3k	Carbon Film	¼	5	20-2332
R29	10k	Carbon Film	¼	5	20-2103
R30	10k	Carbon Film	¼	5	20-2103

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R31	3.3k	Carbon Film	¼	5	20-2332
R32	10k	Carbon Film	¼	5	20-2103
R33	56	Carbon Film	¼	5	20-2560
R34	330	Carbon Film	¼	5	20-2331
R35	100k	Carbon Film	¼	5	20-2104
R36	5 x 10k	DIL Array			20-5534
R37	9 x 2.2k	DIL Array			20-5533
R38	9 x 3.3k	DIL Array			20-5532
R39	9 x 2.2k	DIL Array			20-5533
R40	9 x 3.3k	DIL Array			20-5532
R41	10k	Carbon Film	0.1	5	20-1538
R42	33k	Carbon Film	0.1	5	20-1537
R43	47	Carbon Film	¼	5	20-2470
R44	8.2k	Carbon Film	¼	5	20-2822
R45	27k	Carbon Film	¼	5	20-2273
R46	10k	Carbon Film	¼	5	20-2103
R47	15k	Carbon Film	¼	5	20-2153
R48	10k	Carbon Film	¼	5	20-2103
R49	10k	Carbon Film	¼	5	20-2103
R50	27k	Carbon Film	¼	5	20-2273
R51	27k	Carbon Film	¼	5	20-2273
R52	270k	Carbon Film	¼	5	20-2274
R53	470k	Carbon Film	¼	5	20-2474
R54	270k	Carbon Film	¼	5	20-2274
R55	470k	Carbon Film	¼	5	20-2474
R56	2.2k	Carbon Film	¼	5	20-2222
R57	2.2k	Carbon Film	¼	5	20-2222
R58	2.2k	Carbon Film	¼	5	20-2222
R59	10k	Variable			20-7071
R60	10k	Carbon Film	¼	5	20-2103
R61	100k	Carbon Film	¼	5	20-2104
R62	10k	Carbon Film	¼	5	20-2103
R63	3.3k	Carbon Film	¼	5	20-2332
R64	180	Carbon Film	¼	5	20-2181
Capacitors					
	F		V		
C1	10n	Ceramic	25	-20+80	21-1545
C2	100µ	Electrolytic	25	-10+50	21-0635
C3	10n	Ceramic	25	-20+80	21-1545
C4	10n	Ceramic	25	-20+80	21-1545
C5	6.8µ	Electrolytic	25		21-0720

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
C6	6.8µ	Electrolytic	25		21-0720
C7	100n	Ceramic	12	-20+80	21-1616
C8	10µ	Electrolytic	10		21-0708
C9	1µ	Electrolytic	40		21-0731
C10	4.7µ	Electrolytic	25		21-0723
C11	4.7µ	Electrolytic	25		21-0723
C12	220p	Ceramic	500	10	21-1524
C13	220p	Ceramic	500	10	21-1524
C14	220p	Ceramic	500	10	21-1524
C15	220p	Ceramic	500	10	21-1524
C16	47µ	Electrolytic	6.3		21-0704
C17	100n	Ceramic	12	-20+80	21-1616
C18	100n	Ceramic	12	-20+80	21-1616
C19	100n	Ceramic	12	-20+80	21-1616
C20	1µ	Electrolytic	40		21-0731
C21	220p	Ceramic	500	10	21-1524
C22	100n	Ceramic	12	-20+80	21-1616
C23	100n	Ceramic	12	-20+80	21-1616
C24	47µ	Electrolytic	6.3		21-0704
C25	100µ	Ceramic	12	-20+80	21-1616
C26	47µ	Electrolytic	6.3		21-0704
C27	100n	Ceramic	12	-20+80	21-1616
C28	100n	Ceramic	12	-20+80	21-1616
C29	47µ	Electrolytic	6.3		21-0704
C30	47µ	Electrolytic	40	-10+50	21-0644
C31	1n	Ceramic	500	20	21-1532
C32	10n	Ceramic	25	-20+80	21-1545
C33	100µ	Electrolytic	25	-10+50	21-0635
C34	10n	Ceramic	25	-20+80	21-1545
C35	100µ	Electrolytic	25	-10+50	21-0635
C36	100n	Ceramic	12	-20+80	21-1616
C37	47µ	Electrolytic	6.3		21-0704
C38	100n	Ceramic	12	-20+80	21-1616
C39	47µ	Electrolytic	6.3		21-0704
C40	1n	Ceramic	500	20	21-1532
C41	47µ	Electrolytic	40	-10+50	21-0644
C42	100n	Ceramic	12	-20+80	21-1616
C43	47µ	Electrolytic	6.3		21-0704
C44	100µ	Electrolytic	40		21-0769
C45	10n	Ceramic	25	-20+80	21-1545
C46	100n	Ceramic	12	-20+80	21-1616

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
D3		Not Used			
D4		Not Used			
D5		Silicon (1N4149)			22-1029
D6		Silicon (1N4149)			22-1029
Integrated Circuits					
IC1		74LS125			22-4657
IC2		ZN458B			22-4250
IC3		82S123N (programmed)			22-8521
IC4		ZN428			22-4255
IC5		ZN428			22-4255
IC6		ZN428			22-4255
IC7		74LS138			22-4587
IC8		74LS374			22-4672
IC9		82S123N (programmed)			22-8521
IC10		74LS107			22-4675
IC11		ZN428			22-4255
IC12		ZN428			22-4255
IC13		ZN428			22-4255
IC14		ZN428			22-4255
IC15		ULN 2803A			22-4663
IC16		74LS374			22-4672
IC17		74LS107			22-4675
IC18		74LS221			22-4581
IC19		74LS221			22-4581
IC20		74LS221			22-4581
IC21		74LS367			22-4592
IC22		74LS154			22-4589
IC23		74LS00			22-4531
IC24		74LS04			22-4533
IC25		74LS74			22-4534
IC27		4042			22-4702
IC27		4042			22-4702

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Transistors					
Q1		ZTX450			22-6112
Q2		ZTX450			22-6112
Q3		BC109			22-6041
Q4		BC109			22-6041
Q5		BC109			22-6041
Q6		BC109			22-6041
Q7		ZTX550			22-6113
Q8		BC109			22-6041
Q9		BC109			22-6041
Q10		2N4124			22-6009
Q11		2N4126			22-6010
Q12		ZTX450			22-6112
Q13		ZTX450			22-6112
Q14		ZTX550			22-6113
Q15		BC109			22-6041
Q16		2N4126			22-6010
Q17		MPS-A14			22-6160
Connectors					
PL5		PCB Header, 15-way			17-1029
PL6		PCB Header, 8-way			17-1028
PL7		Connector, 40-way			23-3331
PL8		PCB Header, 16-way			17-1030
PL9		Connector, 50-way			23-3332
PL10		Connector, 50-way			23-3332
PL11		Connector, 40-way			23-3331
PL12		Connector, 6-way			23-3354
PL13		Connector, 12-way			23-3355
SK14		Connector, 32-way			23-5127
SK15		Connector, 32-way			23-5127
SK16		Connector, 24-way			23-5128
SK17		Connector, 24-way			23-5128
		IC Socket, 16-way (IC3 and IC9)			23-3259
Miscellaneous					
X1		Piezo audio indicator			23-9108

PARTS LIST

AUDIO SYSTEM ASSEMBLY 19-1048

Fig 8

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors					
	Ω		W		
R1	1M	Carbon Film	¼	5	20-2105
R2	680	Metal Oxide	½	5	20-3681
R3	100k	Carbon Film	¼	5	20-2104
R4	100	Carbon Film	¼	5	20-2101
R5	1.2k	Carbon Film	¼	5	20-2122
R6	1M	Carbon Film	¼	5	20-2105
R7	1.2k	Carbon Film	¼	5	20-2122
R8	10k	Carbon Film	¼	5	20-2103
R9	10k	Carbon Film	¼	5	20-2103
R10	10k	Carbon Film	¼	5	20-2103
R11	10k	Carbon Film	¼	5	20-2103
R12	100k	Carbon Film	¼	5	20-2104
R13	12k	Carbon Film	¼	5	20-2123
R14	100	Carbon Film	¼	5	20-2101
R15	1.2k	Carbon Film	¼	5	20-2122
R16	100	Carbon Film	¼	5	20-2101
R17	10k	Variable			20-7071
R18	10k	Variable			20-7071
R19	1.2k	Carbon Film	¼	5	20-2122
R20	680k	Carbon Film	¼	5	20-2684
R21	5.6k	Carbon Film	¼	5	20-2562
R22	1M	Carbon Film	¼	5	20-2105
R23	1k	Carbon Film	¼	5	20-2102
R24		Not Used			
R25	18k	Carbon Film	¼	5	20-2183
R26	6.8k	Carbon Film	¼	5	20-2682
R27	5.6k	Carbon Film	¼	5	20-2562
R28	3.3k	Carbon Film	¼	5	20-2332
R29	15k	Carbon Film	¼	5	20-2153
R30	1.5M	Carbon Film	¼	5	20-2155

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R31	100k	Carbon Film	¼	5	20-2104
R32	68k	Carbon Film	¼	5	20-2683
R33	1M	Carbon Film	¼	5	20-2105
R34	100	Carbon Film	¼	5	20-2101
R35	20k	Variable			20-7090
R36	5k	Variable			20-7075
R37	100	Carbon Film	¼	5	20-2101
R38	100k	Carbon Film	¼	5	20-2104
R39	100	Carbon Film	¼	5	20-2101
R40	22k	Carbon Film	¼	5	20-2223
R41		Not Used			
R42	1k	Carbon Film	¼	5	20-2102
R43	1k	Carbon Film	¼	5	20-2102
R44	47k	Carbon Film	¼	5	20-2473
R45	3.3k	Carbon Film	¼	5	20-2332
R46	100	Carbon Film	¼	5	20-2101
R47		Not Used			
R48	100	Carbon Film	¼	5	20-2101
R49	3.3k	Carbon Film	¼	5	20-2332
R50	100k	Carbon Film	¼	5	20-2104
R51		Not Used			
R52	3.3k	Carbon Film	¼	5	20-2332
R53	100k	Carbon Film	¼	5	20-2104
R54	10k	Carbon Film	¼	5	20-2103
R55	47k	Carbon Film	¼	5	20-2473
R56	10k	Carbon Film	¼	5	20-2103
R57	1k	Variable			20-7070
R58	1k	Carbon Film	¼	5	20-2102
R59	10k	Carbon Film	¼	5	20-2103
R60	1M	Carbon Film	¼	5	20-2105
R61	100	Carbon Film	¼	5	20-2101
R62	1.8k	Carbon Film	¼	5	20-2182
R63	5k	Variable			20-7044
R64	560	Carbon Film	¼	5	20-2561
R65	27k	Carbon Film	¼	5	20-2273
R66	27k	Carbon Film	¼	5	20-2273
R67	27k	Carbon Film	¼	5	20-2273
R68	27k	Carbon Film	¼	5	20-2273
R69	100	Carbon Film	¼	5	20-2101
R70	100	Carbon Film	¼	5	20-2101

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R71	820	Carbon Film	¼	5	20-2821
R72	10k	Carbon Film	¼	5	20-2103
R73	10k	Carbon Film	¼	5	20-2103
R74	10k	Carbon Film	¼	5	20-2103
R75	10k	Carbon Film	¼	5	20-2103
R76	100	Carbon Film	¼	5	20-2101
R77	100	Carbon Film	¼	5	20-2101
R78	10k	Variable			20-7071
R79	100k	Carbon Film	¼	5	20-2104
R80	1M	Carbon Film	¼	5	20-2105
R81	27k	Carbon Film	¼	5	20-2273
R82	1k	Variable			20-7070
R83	100k	Carbon Film	¼	5	20-2104
R84	100	Carbon Film	¼	5	20-2101
R85	1.5k	Carbon Film	¼	5	20-2152
R86	1M	Carbon Film	¼	5	20-2105
R87	10k	Carbon Film	¼	5	20-2103
R88	100	Carbon Film	¼	5	20-2101
R89	10k	Variable			20-7071
R90	100	Carbon Film	¼	5	20-2101
R91	100k	Carbon Film	¼	5	20-2104
R92	10k	Carbon Film	¼	5	20-2103
R93	1M	Carbon Film	¼	5	20-2105
R94	1.5k	Carbon Film	¼	5	20-2152
R95	100k	Carbon Film	¼	5	20-2104
R96	100k	Carbon Film	¼	5	20-2104
R97	100	Carbon Film	¼	5	20-2101
R98	1M	Carbon Film	¼	5	20-2105
R99	100k	Carbon Film	¼	5	20-2104
R100	100k	Carbon Film	¼	5	20-2104
R101	680	Metal Oxide	½	5	20-3681
R102	1M	Carbon Film	¼	5	20-2105
R103	10k	Carbon Film	¼	5	20-2103
R104	100k	Carbon Film	¼	5	20-2104
R105	100k	Carbon Film	¼	5	20-2104
R106	1M	Carbon Film	¼	5	20-2105
R107	10k	Carbon Film	¼	5	20-2103
R108	10k	Carbon Film	¼	5	20-2103
R109	100k	Carbon Film	¼	5	20-2104
R110	100	Carbon Film	¼	5	20-2101

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R111	100	Carbon Film	¼	5	20-2101
R112	10k	Carbon Film	¼	5	20-2103
R113	10k	Carbon Film	¼	5	20-2103
R114	12k	Carbon Film	¼	5	20-2123
R115	10k	Variable			20-7071
R116	100k	Carbon Film	¼	5	20-2104
R117	100k	Carbon Film	¼	5	20-2104
R118	10k	Variable			20-7071
R119	680k	Carbon Film	¼	5	20-2684
R120	5.6k	Carbon Film	¼	5	20-2562
R121	18k	Carbon Film	¼	5	20-2183
R122	1k	Carbon Film	¼	5	20-2102
R123	5.6k	Carbon Film	¼	5	20-2562
R124	1M	Carbon Film	¼	5	20-2105
R125	3.3k	Carbon Film	¼	5	20-2332
R126	6.8k	Carbon Film	¼	5	20-2682
R127		Not Used			
R128	1.5M	Carbon Film	¼	5	20-2155
R129	20k	Variable			20-7090
R130	5k	Variable			20-7075
R131	15k	Carbon Film	¼	5	20-2153
R132	100k	Carbon Film	¼	5	20-2104
R133	68k	Carbon Film	¼	5	20-2683
R134	1M	Carbon Film	¼	5	20-2105
R135	100	Carbon Film	¼	5	20-2101
R136	100	Carbon Film	¼	5	20-2101
R137	100k	Carbon Film	¼	5	20-2104
R138	1k	Carbon Film	¼	5	20-2102
R139	1k	Carbon Film	¼	5	20-2102
R140	100	Carbon Film	¼	5	20-2101
R141	22k	Carbon Film	¼	5	20-2223
R142		Not Used			
R143	47k	Carbon Film	¼	5	20-2473
R144	3.3k	Carbon Film	¼	5	20-2332
R145		Not Used			
R146	3.3k	Carbon Film	¼	5	20-2332
R147	100	Carbon Film	¼	5	20-2101
R148		Not Used			
R149	100	Carbon Film	¼	5	20-2101
R150	3.3k	Carbon Film	¼	5	20-2332

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R151	100k	Carbon Film	¼	5	20-2104
R152	100k	Carbon Film	¼	5	20-2104
R153		Not Used			
R154	47k	Carbon Film	¼	5	20-2473
R155		Not Used			
R156		Not Used			
R157	1k	Carbon Film	¼	5	20-2102
R158	1k	Carbon Film	0.1	5	20-1521
R159	1M	Carbon Film	¼	5	20-2105
R160	100	Carbon Film	¼	5	20-2101
R161	27k	Carbon Film	¼	5	20-2273
R162	27k	Carbon Film	¼	5	20-2273
R163	27k	Carbon Film	¼	5	20-2273
R164	27k	Carbon Film	¼	5	20-2273
R165	1.2k	Carbon Film	¼	5	20-2122
R166	1k	Variable			20-7070
R167	27k	Carbon Film	¼	5	20-2273
R168	560	Carbon Film	¼	5	20-2561
R169	100	Carbon Film	¼	5	20-2101
R170	100	Carbon Film	¼	5	20-2101
R171	820	Carbon Film	¼	5	20-2821
R172	150k	Carbon Film	¼	5	20-2154
R173	10k	Carbon Film	¼	5	20-2103
R174	10k	Carbon Film	¼	5	20-2103
R175	10k	Carbon Film	¼	5	20-2103
R176	10k	Carbon Film	¼	5	20-2103
R177	100	Carbon Film	¼	5	20-2101
R178	100k	Carbon Film	¼	5	20-2104
R179	100k	Carbon Film	¼	5	20-2104
R180	100	Carbon Film	¼	5	20-2101
R181	10k	Variable			20-7071
R182	10k	Carbon Film	¼	5	20-2103
R183	100k	Carbon Film	¼	5	20-2104
R184	1M	Carbon Film	¼	5	20-2105
R185	100k	Carbon Film	¼	5	20-2104
R186	100	Carbon Film	¼	5	20-2101
R187	3.3k	Carbon Film	¼	5	20-2332
R188	3.3k	Carbon Film	¼	5	20-2332
R189	3.3k	Carbon Film	¼	5	20-2332
R190	3.3k	Carbon Film	¼	5	20-2332

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R191	9x100k	DIL Array			20-5522
R192	100k	Carbon Film	¼	5	20-2104
R193	100	Carbon Film	¼	5	20-2101
R194	100	Carbon Film	¼	5	20-2101
R195	100k	Carbon Film	¼	5	20-2104
R196	100k	Carbon Film	¼	5	20-2104
R197	100k	Carbon Film	¼	5	20-2104
R198	100k	Carbon Film	¼	5	20-2104
R199	100k	Carbon Film	¼	5	20-2104
R200	100k	Carbon Film	¼	5	20-2104
R201	100k	Carbon Film	¼	5	20-2104
Capacitors	F		V		
C1	47µ	Electrolytic	16		21-0596
C2	47µ	Electrolytic	16		21-0596
C3	47µ	Electrolytic	16		21-0596
C4	47µ	Electrolytic	16		21-0596
C5	47µ	Electrolytic	16		21-0596
C6	47µ	Electrolytic	16		21-0596
C7	10n	Ceramic	25	-20+80	21-1545
C8	10n	Ceramic	25	-20+80	21-1545
C9	10n	Ceramic	25	-20+80	21-1545
C10	10n	Ceramic	25	-20+80	21-1545
C11	10n	Ceramic	25	-20+80	21-1545
C12	1µ	Electrolytic	25		21-0719
C13	47µ	Electrolytic	16		21-0596
C14	47µ	Electrolytic	16		21-0596
C15		Not Used			
C16	1µ	Polyester	100	10	21-4569
C17	39p	Ceramic	63	2	21-1687
C18	33µ	Electrolytic	25	20	21-0782
C19	47µ	Electrolytic	16		21-0596
C20	47µ	Electrolytic	16		21-0596
C21	47µ	Electrolytic	16		21-0596
C22	47µ	Electrolytic	16		21-0596
C23	47µ	Electrolytic	16		21-0596
C24		Not Used			
C25		Not Used			

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
C26	33µ	Electrolytic	25	20	21-0782
C27	47µ	Electrolytic	16		21-0596
C28	10µ	Electrolytic	16		21-0775
C29	1µ	Polyester	100	10	21-4569
C30	47µ	Electrolytic	16		21-0596
C31	10n	Ceramic	25	-20+80	21-1545
C32	47µ	Electrolytic	16		21-0596
C33	47µ	Electrolytic	16		21-0596
C34	47µ	Electrolytic	16		21-0596
C35	47µ	Electrolytic	16		21-0596
C36	47µ	Electrolytic	16		21-0596
C37	47µ	Electrolytic	16		21-0596
C38	22p	Ceramic	63	2	21-1684
C39	47µ	Electrolytic	16		21-0596
C40	47µ	Electrolytic	16		21-0596
C41	47µ	Electrolytic	16		21-0596
C42	330p	Ceramic	63	2	21-1698
C43	47µ	Electrolytic	16		21-0596
C44	47µ	Electrolytic	16		21-0596
C45	2.7n	Ceramic	500	20	21-1537
C46	47µ	Electrolytic	16		21-0596
C47	100µ	Electrolytic	6.3		21-0774
C48	100µ	Electrolytic	6.3		21-0774
C49	47µ	Electrolytic	16		21-0596
C50	10n	Ceramic	25	-20+80	21-1545
C51	10n	Ceramic	25	-20+80	21-1545
C52	10n	Ceramic	25	-20+80	21-1545
C53	10n	Ceramic	25	-20+80	21-1545
C54	47µ	Electrolytic	16		21-0596
C55	47µ	Electrolytic	16		21-0596
C56	47µ	Electrolytic	16		21-0596
C57	47µ	Electrolytic	16		21-0596
C58	47µ	Electrolytic	16		21-0596
C59	47µ	Electrolytic	16		21-0596
C60	10n	Ceramic	25	-20+80	21-1545
C61	10n	Ceramic	25	-20+80	21-1545
C62	10n	Ceramic	25	-20+80	21-1545
C63	10n	Ceramic	25	-20+80	21-1545
C64	10n	Ceramic	25	-20+80	21-1545
C65	47µ	Electrolytic	16		21-0596

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
C66	1µ	Electrolytic	25		21-0719
C67		Not Used			
C68	47µ	Electrolytic	16		21-0596
C69	1µ	Polyester	100	10	21-4569
C70	33µ	Electrolytic	25	20	21-0782
C71	47µ	Electrolytic	16		21-0596
C72	47µ	Electrolytic	16		21-0596
C73	47µ	Electrolytic	16		21-0596
C74	47µ	Electrolytic	16		21-0596
C75	47µ	Electrolytic	16		21-0596
C76	47µ	Electrolytic	16		21-0596
C77		Not Used			
C78		Not Used			
C79	47µ	Electrolytic	16		21-0596
C80	33µ	Electrolytic	25	20	21-0782
C81	100n	Ceramic	12	-20+80	21-1616
C82	10µ	Electrolytic	16		21-0775
C83	1µ	Polyester	100	10	21-4569
C84	47µ	Electrolytic	16		21-0596
C85	10n	Ceramic	25	-20+80	21-1545
C86	47µ	Electrolytic	16		21-0596
C87	47µ	Electrolytic	16		21-0596
C88	10n	Ceramic	25	-20+80	21-1545
C89	47µ	Electrolytic	16		21-0596
C90	47µ	Electrolytic	16		21-0596
C91	47µ	Electrolytic	16		21-0596
C92	47µ	Electrolytic	16		21-0596
C93	15p	Ceramic	63	2	21-1682
C94	47µ	Electrolytic	16		21-0596
C95	47µ	Electrolytic	16		21-0596
C96	100n	Ceramic	12	-20+80	21-1616
C97	100n	Ceramic	12	-20+80	21-1616
C98	10n	Ceramic	25	-20+80	21-1545
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
D3		Silicon (1N4149)			22-1029
D4		Silicon (1N4149)			22-1029
D5		Silicon (1N4149)			22-1029

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
D6		Schottky barrier (5082.2826)			22-1073
D7		Silicon (1N4149)			22-1029
D8		Silicon (1N4149)			22-1029
D9		Silicon (1N4149)			22-1029
D10		Schottky barrier (5082.2826)			22-1073
D11		Silicon (1N4149)			22-1029
D12		Voltage regulator (BZX79C5V1)			22-1857
D13		Silicon (1N4149)			22-1029
D14		Silicon (1N4149)			22-1029
D15		Silicon (1N4149)			22-1029
D16		Silicon (1N4149)			22-1029
D17		Silicon (1N4149)			22-1029
D18		Silicon (1N4149)			22-1029
D19		Silicon (1N4149)			22-1029
D20		Hot Carrier (5082.2811)			22-1033
D21		Silicon (1N4149)			22-1029
D22		Silicon (1N4149)			22-1029
D23		Silicon (1N4149)			22-1029
D24		Schottky barrier (5820.2826)			22-1073
D25		Silicon (1N4149)			22-1029
D26		Schottky barrier (5820.2826)			22-1073
D27		Hot Carrier (5082.2811)			22-1033
D28		Voltage regulator (BZX79C5V1)			22-1857
D29		Silicon (1N4149)			22-1029
D30		Silicon (1N4149)			22-1029
D31		Silicon (1N4149)			22-1029
D32		Silicon (1N4149)			22-1029
D33		Silicon (1N4149)			22-1029
D34		Hot Carrier (5082.2811)			22-1033

Integrated Circuits

IC1		HEF4104			22-4764
IC2		7523			22-4766
IC3		HEF4104			22-4764
IC4		TL081			22-4229
IC5		DG200CJ			22-4744
IC6		TL081			22-4229
IC7		TL082			22-4240
IC8		TL081			22-4229
IC9		TL082			22-4240
IC10		4071			22-4716

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
IC11		TL082			22-4240
IC12		TL081			22-4229
IC13		TL082			22-4240
IC14		DG201CJ			22-4765
IC15		7541			22-4767
IC16		TL081			22-4229
IC17		TL082			22-4240
IC18		TL082			22-4240
IC19		TL082			22-4240
IC20		4071			22-4716
IC21		DG201CJ			22-4765
IC22		DG201CJ			22-4765
IC23		TL081			22-4229
IC24		DG200CJ			22-4744
IC25		DG201CJ			22-4765
IC26		DG201CJ			22-4765
IC27		DG200CJ			22-4744
IC28		TL082			22-4240
IC29		4042			22-4702
IC30		DG200CJ			22-4744
IC31		4049			22-4719
IC32		4011			22-4700
IC33		DG200CJ			22-4744
IC34		TL081			22-4229
IC35		4042			22-4702
IC36		4042			22-4702
IC37		DG201CJ			22-4765
IC38		4071			22-4716
IC39		4049			22-4719
IC40		DG201CJ			22-4765
IC41		74LS138			22-4587
IC42		4071			22-4716
IC43		4011			22-4700
IC44		DG201CJ			22-4765
IC45		4042			22-4702
IC46		4042			22-4702
IC47		4042			22-4702
IC48		4042			22-4702
IC49		74LS138			22-4587
IC50		74LS74			22-4534

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Transistors					
Q1		E108			22-6111
Q2		BC107			22-6068
Q3		BFX48			22-6110
Q4		Not Used			
Q5		2N4416			22-6040
Q6		Not Used			
Q7		Not Used			
Q8		Not Used			
Q9		Not Used			
Q10		BC109			22-6041
Q11		BC109			22-6041
Q12		BC109			22-6041
Q13		BC109			22-6041
Q14		BC107			22-6068
Q15		E108			22-6111
Q16		BC107			22-6068
Q17		E108			22-6111
Q18		E108			22-6111
Q19		BFX48			22-6110
Q20		E108			22-6111
Q21		BC107			22-6068
Q22		BFX48			22-6110
Q23		E108			22-6111
Q24		BC107			22-6068
Q25		BFX48			22-6110
Q26		Not Used			
Q27		2N4416			22-6040
Q28		Not Used			
Q29		Not Used			
Q30		Not Used			
Q31		Not Used			
Q32		BC109			22-6041
Q33		BC109			22-6041
Q34		BC109			22-6041
Q35		BC109			22-6041
Q36		BFX48			22-6110
Q37		E108			22-6111
Q38		BC107			22-6068

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Connectors					
PL24		Connector, 50-way			23-3332
PL25		Connector, 40-way			23-3331
PL26		Connector, 50-way			23-3340
PL27		Connector, 40-way			23-3339
SK18		Coaxial receptacle			23-3338
SK19		Coaxial receptacle			23-3338
SK20		Coaxial receptacle			23-3338
SK21		Coaxial receptacle			23-3338
SK22		Coaxial receptacle			23-3338
SK23		Coaxial receptacle			23-3338
		Coaxial cable assembly			15-0630

PARTS LIST

NON-VOLATILE MEMORY ASSEMBLY 19-1049

Fig 10

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors	Ω		W		
R1	10k	Carbon Film	¼	5	20-2103
R2	9 x 3.3k	DIL Array			20-5532
R3	1k	Carbon Film	¼	5	20-2102
R4	1.5k	Carbon Film	¼	5	20-2152
R5		Not Used			
R6	9 x 10k	DIL Array			20-5521
R7	9 x 3.3k	DIL Array			20-5532
R8	1k	Carbon Film	¼	5	20-2102
R9	1k	Carbon Film	¼	5	20-2102
R10	1k	Carbon Film	0.1	5	20-1521
R11	15k	Carbon Film	¼	5	20-2153
R12	2.2M	Carbon Film	¼	10	20-2225
R13	150	Carbon Film	¼	5	20-2151
R14	1.8k	Carbon Film	0.1	5	20-1541
R15	10k	Carbon Film	0.1	5	20-1538
R16	820k	Carbon Film	0.1	5	20-1581
R17	500k	Variable			20-7100
R18	820k	Carbon Film	0.1	5	20-1581
R19	22M	Metal Glaze	½	5	20-7313
R20	3.3k	Carbon Film	0.1	5	20-1537
R21	2.2k	Carbon Film	¼	5	20-2222
R22	2.2k	Carbon Film	¼	5	20-2222
R23	10k	Carbon Film	0.1	5	20-1538
Capacitors	F				
C1	100n	Ceramic	12	-20+80	21-1616
C2	100n	Ceramic	12	-20+80	21-1616
C3	47µ	Electrolytic	6.3		21-0704
C4	100n	Ceramic	12	-20+80	21-1616
C5	100n	Ceramic	12	-20+80	21-1616

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
C6	47µ	Electrolytic	6.3		21-0704
C7	100n	Ceramic	12	-20+80	21-1616
C8	100n	Ceramic	12	-20+80	21-1616
C9	47µ	Electrolytic	6.3	20	21-0773
C10	100n	Ceramic	12	-20+80	21-1616
C11	100n	Ceramic	12	-20+80	21-1616
C12	33n	Ceramic	100	10	21-1547
C13	100n	Ceramic	12	-20+80	21-1616
C14	10n	Ceramic	25	-20+80	21-1545
C15	100n	Ceramic	12	-20+80	21-1616
C16	330p	Ceramic	500	10	21-1526
C17	1n	Silver Mica	200	2	21-3061
C18	10µ	Electrolytic	10		21-0708
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
D3		Silicon (1N4149)			22-1029
Integrated Circuits					
IC1		6514			22-8204
IC2		4521			22-4769
IC3		6514			22-8204
IC4		6514			22-8204
IC5		74LS74			22-4534
IC6		Not Used			
IC7		6514			22-8204
IC8		74LS14			22-4570
IC9		8211			22-4257
IC10		Not Used			
IC11		Not Used			
IC12		74LS00			22-4531
IC13		Not Used			
IC14		Not Used			
IC15		7442			22-4058

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
IC16		Not Used			
IC17		Not Used			
IC18		74LS27			22-4549
IC19		74LS244			22-4583
IC20		74LS245			22-4584
IC21		Not Used			
IC22		74LS125			22-4657
IC23		555			22-4206
Transistors					
Q1		ZTX313L			22-6079
Q2		Not Used			
Q3		2N4126			22-6010
Q4		BC109			22-6041
Q5		2N4126			22-6010
Miscellaneous					
		IC Socket, 18-way			23-3295
B1		Battery			23-2512

PARTS LIST

GPIB ASSEMBLY 19-1050

Fig 12

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors	Ω		W		
R1	1k	Carbon Film	¼	5	20-2102
R2	9 x 3.3k	DIL Array			20-5532
R3	3.3k	Carbon Film	¼	5	20-2332
R4	56	Carbon Film	¼	5	20-2560
R5	9 x 3.3k	DIL Array			20-5532
R6	56	Carbon Film	¼	5	20-2560
Capacitors	F		V		
C1	10n	Ceramic	25	-20+80	21-1545
C2	47µ	Electrolytic	16		21-0596
C3	47µ	Electrolytic	16		21-0596
C4	100n	Ceramic	12	-20+80	21-1616
C5	100n	Ceramic	12	-20+80	21-1616
C6	100n	Ceramic	12	-20+80	21-1616
C7	100n	Ceramic	12	-20+80	21-1616
C8	10n	Ceramic	25	-20+80	21-1545
C9	100n	Ceramic	12	-20+80	21-1616
C10	10n	Ceramic	25	-20+80	21-1545
C11	100n	Ceramic	12	-20+80	21-1616
Integrated Circuits					
IC1		74LS240			22-4588
IC2		3447			22-8304
IC3		3447			22-8304
IC4		74LS02			22-4532
IC5		68488			22-8305

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
IC6		74LS30			22-4597
IC7		74LS10			22-4557
IC8		74LS04			22-4533
IC9		74LS125			22-4657
IC10		74LS74			22-4534
IC11		74LS30			22-4597
IC12		4066			22-4761
IC13		74LS138			22-4587
IC14		74LS10			22-4557
IC15		74LS74			22-4534
IC16		74LS86			22-4566
IC17		Programmed ROM			22-8553
IC18		74LS245			22-4584
Inductors					
	H				
L1	1µ	Choke, sub-miniature		10	23-7008
Miscellaneous					
PL68		PCB header, 26-way			23-3394
		IC Socket 40-way (IC5)			23-3246
		IC Socket 24-way (IC17)			23-3245

PARTS LIST

PROCESSOR ASSEMBLY 19-1051

Fig 14

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors					
	Ω		W		
R1	10k	Carbon Film	¼	5	20-2103
R2	9 x 3.3k	DIL Array			20-5532
R3	9 x 3.3k	DIL Array			20-5532
R4	3.3k	Carbon Film	¼	5	20-2332
R5	100k	Carbon Film	¼	5	20-2104
R6	100	Carbon Film	¼	5	20-2101
R7	3.3k	Carbon Film	¼	5	20-2332
R8	9 x 10k	DIL Array			20-5521
R9	560	Carbon Film	¼	5	20-2561
R10	4.7k	Carbon Film	¼	5	20-2472
R11	10k	Variable			20-7071
R12	10k	Carbon Film	¼	5	20-2103
R13	10k	Carbon Film	¼	5	20-2103
R14	3.3k	Carbon Film	¼	5	20-2332
R15	3.3k	Carbon Film	¼	5	20-2332
R16	12k	Carbon Film	¼	5	20-2123
R17	12k	Carbon Film	¼	5	20-2123
R18	10k	Carbon Film	¼	5	20-2103
R19	10k	Carbon Film	¼	5	20-2103
R20	9 x 10k	DIL Array			20-5521
R21	9 x 10k	DIL Array			20-5521
R22	9 x 100k	DIL Array			20-5522
R23	9 x 10k	DIL Array			20-5521
R24	3.3k	Carbon Film	¼	5	20-2332
R25	9 x 10k	DIL Array			20-5521
R26	10k	Carbon Film	¼	5	20-2103
R27	10k	Carbon Film	¼	5	20-2103
R28	9 x 10k	DIL Array			20-5521
R29	220	Carbon Film	¼	5	20-2221

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Capacitors					
	F				
C1	100n	Ceramic	12	-20+80	21-1616
C2	100n	Ceramic	12	-20+80	21-1616
C3	100n	Ceramic	12	-20+80	21-1616
C4	100n	Ceramic	12	-20+80	21-1616
C5	100n	Ceramic	12	-20+80	21-1616
C6	100n	Ceramic	12	-20+80	21-1616
C7	100n	Ceramic	12	-20+80	21-1616
C8	27p	Ceramic	500	10	21-1513
C9	27p	Ceramic	500	10	21-1513
C10	47µ	Electrolytic	6.3		21-0704
C11	100n	Ceramic	12	-20+80	21-1616
C12	100n	Ceramic	12	-20+80	21-1616
C13	100n	Ceramic	12	-20+80	21-1616
C14	68p	Ceramic	63	2	21-1690
C15	100n	Ceramic	12	-20+80	21-1616
C16	100n	Ceramic	12	-20+80	21-1616
C17	100n	Ceramic	12	-20+80	21-1616
C18	22p	Ceramic	500	10	21-1512
C19	22p	Ceramic	500	10	21-1512
C20	100n	Ceramic	12	-20+80	21-1616
C21	100n	Ceramic	12	-20+80	21-1616
C22	100n	Ceramic	12	-20+80	21-1616
C23	100n	Ceramic	12	-20+80	21-1616
C24	100n	Ceramic	12	-20+80	21-1616
C25	4.7µ	Electrolytic	25		21-0723
C26	100n	Ceramic	12	-20+80	21-1616
C27	100n	Ceramic	12	-20+80	21-1616
C28	47µ	Electrolytic	6.3		21-0704
C29	100n	Ceramic	12	-20+80	21-1616
Diodes					
D1		Hot Carrier (5082.2811)			22-1033
D2		Hot Carrier (5082.2811)			22-1033
LP1		LED, red (MV 57641)			26-5025

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Integrated Circuits					
IC1		74LS05			22-4553
IC2		74LS05			22-4553
IC3		74LS377			22-4568
IC4		2716 (programmed)			22-8554
IC5		2716 (programmed)			22-8555
IC6		2716 (programmed)			22-8556
IC7		2716 (programmed)			22-8557
IC8		2716 (programmed)			22-8558
IC9		2716 (programmed)			22-8559
IC10		2716 (programmed)			22-8560
IC11		2716 (programmed)			22-8561
IC12		2716 (programmed)			22-8562
IC13		MK4118-4			22-8202
IC14		4516			22-4757
IC15		74LS244			22-4583
IC16		74LS33			22-4661
IC17		74LS154			22-4589
IC18		74LS74			22-4534
IC19		74LS123			22-4547
IC20		40106			22-4756
IC21		74LS04			22-4533
IC22		74LS125			22-4657
IC23		74LS154			22-4589
IC24		74LS133			22-4662
IC25		74LS244			22-4583
IC26		6802			22-8302
IC27		74LS245			22-4584
IC28		4516			22-4757
IC29		74LS240			22-4588
IC30		74LS240			22-4588
IC31		74LS244			22-4583
IC32		74LS244			22-4583
IC33		74LS240			22-4588
IC34		74LS37			22-4671
IC35		74LS244			22-4583

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
IC36		74LS00			22-4531
IC37		74LS30			22-4597
IC38		74LS09			22-4596
IC39		74LS33			22-4661
IC40		74LS33			22-4661
IC41		40106			22-4756
IC42		74LS244			22-4583
IC43		74LS33			22-4661
IC44		74LS245			22-4584
IC45		74LS154			22-4589
Transistors					
Q1		2N4126			22-6010
Q2		2N4126			22-6010
Q3		BC109			22-6041
Miscellaneous					
		IC Socket, 24-way			23-3245
		IC Socket, 40-way			23-3246
		IC Socket, 20-way			23-3296
S2		Switch, DIL			23-4102
XL1	4 MHz	Crystal			23-9095

PARTS LIST

GPIB CONNECTOR ASSEMBLY 19-1053

Fig 16

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors	Ω		W		
R1	100	Carbon Film	¼	5	20-2101
R2	100	Carbon Film	¼	5	20-2101
Capacitors					
C1	10n	Ceramic	25	-20+80	21-1545
C2	10n	Ceramic	25	-20+80	21-1545
Switches					
S3		Switch, DPDT			23-4099
S4		Switch, 6 x SPST, DIL			23-4102
Relays					
RLA		DIL, 150 Ω coil with protection diode			23-7526
RLB		DIL, 150 Ω coil with protection diode			23-7526
Connectors					
SK68		Cable Assembly			10-2848
SK79		IEEE 488 GPIB connector			23-3314

PARTS LIST

POWER SUPPLY SYSTEM

Fig 20

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
REAR PANEL ASSEMBLY 11-1530					
Thermistor					
TH1		Thermistor, PTC (YK080TC)			22-3004
Integrated Circuits					
IC1		7918			22-4259
IC2		7905			22-4258
Transistors					
Q1		BDT91			22-6152
Q2		BDT91			22-6152
Q3		BDT92			22-6153
Q4		BDT92			22-6153
Q5		BDT92			22-6153
Q6		BDT92			22-6153
Q7		BDT92			22-6153
Power Input Connector					
		AC power plug, filter and fuseholder			23-3294
FS1		Fuselink 4 AT (90 V to 132 V operation)			23-0061
		Fuselink 2 AT (198 V to 264 V operation)			23-0036
POWER UNIT CHASSIS ASSEMBLY 11-1537					
Cable Assemblies					
		Cable assembly			10-2802
PL12, PL13		Cable assembly			10-2803
Transformer					
T1		Power transformer			17-4098

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
Resistors	Ω		W		
R1	270	Metal Oxide	½	5	20-3271
R2	1.8k	Metal Oxide	½	5	20-3182
Capacitors	F		V		
C1	6800µ	Electrolytic	40		21-0674
C2	10000µ	Electrolytic	16		21-0669
C3	10000µ	Electrolytic	25		21-0671
C4	6800µ	Electrolytic	40		21-0674
C5	22000µ	Electrolytic	25		21-0673
C6	68000µ	Electrolytic	10		21-0664
C7	3300µ	Electrolytic	16		21-0666
Diodes					
D1		Bridge rectifier (VH248)			22-1662
D2		Bridge rectifier (VH148)			22-1663
D3		Bridge rectifier (VH148)			22-1663
D4		Bridge rectifier (VH248)			22-1662
D5		Bridge rectifier (VK148)			22-1663
D6		Rectifier (VSK3030S)			22-1616
D7		Rectifier (VSK3030S)			22-1616
D8		Rectifier (1N4002)			22-1602
D9		Rectifier (1N4002)			22-1602
D10		Bridge Rectifier (VH248)			22-1662
D11		Voltage regulator (1N2970)			22-1846
D12		Voltage regulator (Z3B18R)			22-1858
D13		Voltage regulator (Z3B6.2R)			22-1852
D14		Voltage regulator (Z3B6.2R)			22-1852
D15		Voltage regulator (Z3B6.2R)			22-1852
POWER SUPPLY INTERCONNECT ASSEMBLY 19-1058					
Resistors	Ω		W		
R1	0.1	Wire Wound	2.5	10	20-5048
R2	33	Wire Wound	2.5	5	20-5000
R3	0.1	Wire Wound	2.5	10	20-5048
R4	150	Wire Wound	2.5	5	20-5077
R5	390	Wire Wound	2.5	5	20-5065

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R6	0.18	Wire Wound	2.5	5	20-5076
R7	0.047	Wire Wound	2.5	5	20-5075
R8	68	Wire Wound	6	5	20-5063
R9	0.047	Wire Wound	2.5	5	20-5075
R10	22	Wire Wound	2.5	5	20-5078
R11	0.047	Wire Wound	2.5	5	20-5075
R12	22	Wire Wound	2.5	5	20-5078
R13	0.1	Wire Wound	2.5	10	20-5048
R14	33	Wire Wound	2.5	5	20-5000
Capacitors					
	F		V		
C1	1µ	Electrolytic	40		21-0731
C2	4.7µ	Electrolytic	25		21-0723
C3	10µ	Electrolytic	16		21-0716
C4	10µ	Electrolytic	16		21-0716
Diodes					
D1		Silicon (1N4002)			22-1602
Fuses					
FS1		Fuselink 2A			23-0008
FS2		Fuselink 2A			23-0008
FS3		Fuselink 2A			23-0008
FS4		Fuselink 1.5A			23-0007
FS5		Fuselink 3A			23-0009
FS6		Fuselink 3A			23-0009
FS7		Fuselink 3A			23-0009
FS8		Fuselink 2A			23-0008
FS9		Fuselink 0.5A			23-0004
		Fuseholder for FS1-FS9			23-0039
Connectors					
SK71		Connector, 32-way			23-3342
		Bead, mounting, ceramic			23-9119

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
POWER SUPPLY CONTROL ASSEMBLY 19-1059					
Resistors					
	Ω		W		
R1	2.7k	Carbon Film	¼	5	20-2272
R2	4.7k	Carbon Film	¼	5	20-2472
R3	4 x 1k	Variable			20-7101
R4	3.9k	Carbon Film	¼	5	20-2392
R5	220	Carbon Film	¼	5	20-2221
R6	4.7k	Carbon Film	¼	5	20-2472
R7	56k	Carbon Film	¼	5	20-2563
R8	47	Carbon Film	¼	5	20-2470
R9	680	Carbon Film	¼	5	20-2681
R10	2.7k	Carbon Film	¼	5	20-2272
R11	4.7k	Carbon Film	¼	5	20-2472
R12	10k	Carbon Film	¼	5	20-2103
R13	2.7k	Carbon Film	¼	5	20-2272
R14	4.7k	Carbon Film	¼	5	20-2472
R15	1.5k	Carbon Film	¼	5	20-2152
R16	2.2k	Carbon Film	¼	5	20-2222
R17	220	Carbon Film	¼	5	20-2221
R18	2.7k	Carbon Film	¼	5	20-2272
R19	22k	Carbon Film	¼	5	20-2223
R20	56k	Carbon Film	¼	5	20-2563
R21	47	Carbon Film	¼	5	20-2470
R22	2.7k	Carbon Film	¼	5	20-2272
R23	390	Carbon Film	¼	5	20-2391
R24	2.7k	Carbon Film	¼	5	20-2272
R25	470	Carbon Film	¼	5	20-2471
R26	1.2k	Metal Oxide	½	5	20-3122
R27	1.2k	Metal Oxide	¼	2	20-4024
R28	1.5k	Metal Oxide	¼	1	20-4038
R29	2.7k	Carbon Film	¼	5	20-2272
R30	2.7k	Carbon Film	¼	5	20-2272
R31	27k	Carbon Film	¼	5	20-2273
R32	6.8k	Carbon Film	¼	5	20-2682
R33	56k	Carbon Film	¼	5	20-2563
R34	68	Carbon Film	¼	5	20-2680
R35	4.7k	Carbon Film	¼	5	20-2472

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R36	27k	Carbon Film	¼	5	20-2273
R37	56	Carbon Film	¼	5	20-2560
R38	4.7k	Carbon Film	¼	5	20-2472
R39	2.7k	Carbon Film	¼	5	20-2272
R40	2.7k	Carbon Film	¼	5	20-2272
R41	10k	Carbon Film	¼	5	20-2103
R42	4.7k	Carbon Film	¼	5	20-2472
R43	56k	Carbon Film	¼	5	20-2563
R44	47	Carbon Film	¼	5	20-2470
R45	220	Carbon Film	¼	5	20-2221
R46	15k	Carbon Film	¼	5	20-2153
R47	2.7k	Carbon Film	¼	5	20-2272
R48	10k	Carbon Film	¼	5	20-2103
R49	2.7k	Carbon Film	¼	5	20-2272
R50	56k	Carbon Film	¼	5	20-2563
R51	220	Carbon Film	¼	5	20-2221
R52	4.7k	Carbon Film	¼	5	20-2472
R53	47	Carbon Film	¼	5	20-2470
R54	3.9k	Carbon Film	¼	5	20-2392
R55	4 x 1k	Variable			20-7101
R56	4.7k	Carbon Film	¼	5	20-2472
R57	680	Carbon Film	¼	5	20-2681
R58	10k	Carbon Film	¼	5	20-2103
R59	2.7k	Carbon Film	¼	5	20-2272
R60	56k	Carbon Film	¼	5	20-2563
R61	220	Carbon Film	¼	5	20-2221
R62	4.7k	Carbon Film	¼	5	20-2472
R63	47	Carbon Film	¼	5	20-2470
R64	3.9k	Carbon Film	¼	5	20-2392
R65	4.7k	Carbon Film	¼	5	20-2472
R66	680	Carbon Film	¼	5	20-2681
R67	10k	Carbon Film	¼	5	20-2103
R68	2.7k	Carbon Film	¼	5	20-2272
R69	56k	Carbon Film	¼	5	20-2563
R70	220	Carbon Film	¼	5	20-2221
R71	4.7k	Carbon Film	¼	5	20-2472
R72	47	Carbon Film	¼	5	20-2470
R73	3.9k	Carbon Film	¼	5	20-2392
R74	4.7k	Carbon Film	¼	5	20-2472
R75	680	Carbon Film	¼	5	20-2681

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
R76	10k	Carbon Film	¼	5	20-2103
R77	15k	Carbon Film	¼	5	20-2153
R78	1k	Carbon Film	¼	5	20-2102
R79	10k	Carbon Film	¼	5	20-2103
R80	15k	Carbon Film	¼	5	20-2153
R81	8.2k	Carbon Film	¼	5	20-2822
R82	2.7k	Carbon Film	¼	5	20-2272
R83	2.2k	Carbon Film	¼	5	20-2222
R84	470	Carbon Film	¼	5	20-2471
R85	10k	Carbon Film	¼	5	20-2103
R86	10k	Carbon Film	¼	5	20-2103
R87	6.8k	Carbon Film	¼	5	20-2682
R88	2.7k	Carbon Film	¼	5	20-2272
R89	2.2k	Carbon Film	¼	5	20-2222
R90	560	Carbon Film	¼	5	20-2561
R91	3.9k	Carbon Film	¼	5	20-2392
R92	560	Carbon Film	¼	5	20-2561
R93	3.9k	Carbon Film	¼	5	20-2392
R94	1k	Carbon Film	¼	5	20-2102
R95	6.8k	Carbon Film	¼	5	20-2682
R96	1.2k	Carbon Film	¼	5	20-2122
R97	3.9k	Carbon Film	¼	5	20-2392
R98	560	Carbon Film	¼	5	20-2561
R99	2.7k	Carbon Film	¼	5	20-2272
R100	560	Carbon Film	¼	5	20-2561
R101	2.7k	Carbon Film	¼	5	20-2272
R102	1k	Carbon Film	¼	5	20-2102
R103	6.8k	Carbon Film	¼	5	20-2682
R104	22	Carbon Film	¼	5	20-2220
R105	6.8k	Carbon Film	¼	5	20-2682
Capacitors					
	F		V		
C1	100p	Ceramic	500	10	21-1520
C2	22µ	Electrolytic	10		21-0710
C3	100µ	Electrolytic	25		21-0678
C4	100p	Ceramic	500	10	21-1520
C5	22µ	Electrolytic	10		21-0710

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
C6	68µ	Electrolytic	50		21-0694
C7	47µ	Electrolytic	63		21-0593
C8	100p	Ceramic	500	10	21-1520
C9	47µ	Electrolytic	63		21-0593
C10	100p	Ceramic	500	10	21-1520
C11		Not Used			
C12	68µ	Electrolytic	50		21-0694
C13	100p	Ceramic	500	10	21-1520
C14	100µ	Electrolytic	25		21-0678
C15	100p	Ceramic	500	10	21-1520
C16	100µ	Electrolytic	25		21-0678
C17	100p	Ceramic	500	10	21-1520
C18	100µ	Electrolytic	25		21-0678
C19	22µ	Electrolytic	63		21-0752
C20	47µ	Electrolytic	6.3		21-0704
C21	22µ	Electrolytic	10		21-0710
C22	22µ	Electrolytic	10		21-0710

Diodes

D1	Not Used	
D2	Germanium (AAZ15)	22-0007
D3	Silicon (1N4149)	22-1029
D4	Germanium (AAZ15)	22-0007
D5	Not Used	
D6	Germanium (AAZ15)	22-0007
D7	Voltage regulator (BZX79C5V1)	22-1857
D8	Silicon (1N4149)	22-1029
D9	Silicon (1N4149)	22-1029
D10	Silicon (1N4002)	20-1602
D11	Voltage regulator (BZX79C5V1)	22-1857
D12	Silicon (1N4002)	20-1602
D13	Not Used	
D14	Germanium (AAZ15)	20-0007
D15	Silicon (1N4149)	20-1029
D16	Silicon (1N4002)	20-1602
D17	Not Used	
D18	Germanium (AAZ15)	20-0007
D19	Silicon (1N4149)	20-1029
D20	Not Used	

Cct. Ref.	Value	Description	Rat	Tol %	Racal-Dana Part Number
D21		Germanium (AAZ15)			20-0007
D22		Silicon (1N4149)			20-1029
D23		Not Used			
D24		Silicon (1N4149)			20-1029
D25		Germanium (AAZ15)			20-0007
D26		Not Used			
D27		Silicon (1N4149)			20-1029
D28		Silicon (1N4149)			20-1029
LP1		LED array, 8-element, red			26-5019
Integrated Circuits					
IC1		MC3403			22-4262
IC2		MC3403			22-4262
IC3		MC7824			22-4220
IC4		MC3403			22-4262
IC5		MC3403			22-4262
Transistors					
Q1		ZTX550			22-6113
Q2		ZTX550			22-6113
Q3		ZTX450			22-6112
Q4		BDT91			22-6152
Q5		ZTX450			22-6112
Q6		ZTX450			22-6112
Q7		ZTX450			22-6112
Q8		ZTX550			22-6113
Q9		BC109			22-6041
Q10		ZTX450			22-6112
Q11		ZTX450			22-6112
Connector					
PL71		Connector 32-way			23-3341

PARTS LIST

OSCILLATOR SUPPLY FILTER ASSEMBLY 19-1167

Fig 21

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Resistors	Ω		W		
R1	1k	Carbon Film	¼	5	20-2102
R2	8.2k	Carbon Film	¼	5	20-2822
Capacitors	F		V		
C1	470µ	Tantalum	10	20	21-0598
C2	470µ	Tantalum	10	20	21-0598
Transistors					
Q1		2N4126			22-6010
Q2		BDT92			22-6153
Q3		2N4126			22-6010

PARTS LIST

OUTPUT SYSTEM MODULE 11-1532

Fig 23

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Resistors	Ω		W		
R1	5 x 3.3k	DIL Array			20-5531
R2	9 x 100k	DIL Array			20-5522
Capacitors	F		V		
C1	100µ	Electrolytic	6.3		21-0774
C2	47µ	Electrolytic	16		21-0596
C3	47µ	Electrolytic	16		21-0596
C4	100µ	Electrolytic			21-0774
C5	100n	Ceramic	12	-20+80	21-1616
C6	10n	Ceramic	25	-20+80	21-1545
C7	10n	Ceramic	25	-20+80	21-1545
C8	100n	Ceramic	12	-20+80	21-1616
C9	100µ	Electrolytic			21-0774
C10	100µ	Electrolytic			21-0774
C11	100n	Ceramic	12	-20+80	21-1616
C12	100n	Ceramic	12	-20+80	21-1616
Integrated Circuits					
IC1		4042			22-4702
IC2		4042			22-4702
IC3		4042			22-4702
IC4		4042			22-4702
IC5		4042			22-4702
IC6		74LS138			22-4587
Connectors					
PL30		PCB header, 50-way			23-3340
PL31		PCB header, 40-way			23-3339

PARTS LIST

COMB LOOP MODULE 11-1702

Fig 25

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Resistors	Ω		W		
R1	56	Carbon Film	0.1	5	20-1546
R2	4.7k	Carbon Film	0.1	5	20-1542
R3	47k	Carbon Film	0.1	5	20-1572
R4	3.3k	Carbon Film	0.1	5	20-1537
R5	47	Carbon Film	0.1	5	20-1531
R6	47	Carbon Film	0.1	5	20-1531
R7	56	Carbon Film	0.1	5	20-1546
R8	82k	Carbon Film	0.1	5	20-1570
R9	18k	Carbon Film	0.1	5	20-1575
R10	5 x 10k	SIL Array			20-5534
R11	47	Carbon Film	0.1	5	20-1531
R12		Not Used			
R13	22k	Carbon Film	0.1	5	20-1563
R14	100k	Carbon Film	0.1	5	20-1551
R15	5 x 47k	SIL Array			20-5557
R16	4.7k	Metal Oxide	¼	1	10-4075
R17	12k	Metal Oxide	¼	2	20-4067
R18	330	Carbon Film	0.1	5	20-1517
R19	12k	Metal Oxide	¼	2	20-4067
R20	1.5k	Metal Oxide	¼	1	20-4083
R21	47k	Carbon Film	0.1	5	20-1572
R22	4.7k	Metal Oxide	¼	1	20-4075
R23	1.5k	Metal Oxide	¼	1	20-4038
R24	56	Carbon Film	¼	5	20-2560
R25	56	Carbon Film	0.1	5	20-1546
R26	2 x 100k	Variable			20-7076
R27	4 x 100k	Variable			20-7077
R28	4 x 100k	Variable			20-7077
R29	10k	Metal Oxide	¼	1	20-4033
R30	10k	Metal Oxide	¼	1	20-4033
R31	56k	Carbon Film	0.1	5	20-1574
R32	82k	Carbon Film	0.1	5	20-1570
R33	100k	Carbon Film	0.1	5	20-1551
R34	100k	Carbon Film	0.1	5	20-1551
R35	68k	Carbon Film	0.1	5	20-1577

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
R36	82k	Carbon Film	0.1	5	20-1570
R37	82k	Carbon Film	0.1	5	20-1570
Capacitors					
	F		W		
C1	10n	Ceramic	25	-20+80	21-1545
C2	100n	Ceramic	12	-20+80	21-1616
C3	100n	Ceramic	12	-20+80	21-1616
C4	100n	Ceramic	12	-20+80	21-1616
C5	22n	Ceramic	25	-20+80	21-1546
C6	22n	Ceramic	25	-20+80	21-1546
C7	6.8µ	Electrolytic	25		21-0720
C8	47µ	Electrolytic	6.3		21-0704
C9	47µ	Electrolytic	6.3		21-0704
C10	47µ	Electrolytic	6.3		21-0704
C11	15µ	Electrolytic	16		21-0732
C12	15µ	Electrolytic	16		21-0732
C13	10n	Ceramic	25	-20+80	21-1545
C14	10n	Ceramic	25	-20+80	21-1545
C15	10n	Ceramic	25	-20+80	21-1545
C16	6.8µ	Electrolytic	25		21-0720
C17	10n	Ceramic	25	-20+80	21-1545
C18	47µ	Electrolytic	6.3		21-0704
C19	15µ	Electrolytic	16		21-0732
C20	10n	Ceramic	25	-20+80	21-1545
C21	15µ	Electrolytic	16		21-0732
C22	100n	Ceramic	12	-20+80	21-1616
C23	47µ	Electrolytic	6.3		21-0704
C24	47µ	Electrolytic	6.3		21-0704
C25	100n	Ceramic	12	-20+80	21-1616
C26	10n	Ceramic Chip		20	21-1801
C27	10n	Ceramic Chip		20	21-1801
C28	10n	Ceramic Chip		20	21-1801
C29	10n	Ceramic Chip		20	21-1801
C30	10n	Ceramic Chip		20	21-1801
C31	10n	Ceramic Chip		20	21-1801
C32	10n	Ceramic Chip		20	21-1801
C33	10n	Ceramic Chip		20	21-1801
C34	10n	Ceramic Chip		20	21-1801
C35	10n	Ceramic Chip		20	21-1801

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
C36	330p	Ceramic	500	10	21-1526
C37	47µ	Electrolytic	6.3		21-0704
C38	330p	Ceramic	500	10	21-1526
C39	1n	Ceramic Chip		10	21-1800
C40	270p	Ceramic	500	10	21-1525
C41	270p	Ceramic	500	10	21-1525
C42	6.8µ	Electrolytic	25		21-0720
C43	47µ	Electrolytic	6.3		21-0704
C473	15µ	Electrolytic	16		21-0732
Diodes					
D22		Silicon (1N4149)			22-1029
Integrated Circuits					
IC1		TL082			22-4240
IC2		ZN458B			22-4250
IC3		4067			22-4762
IC4		7406			22-4062
IC5		ZN458B			22-4250
IC6		7533			22-4768
IC7		Programmed ROM			22-8549
IC8		TL084			22-4266
IC9		Programmed ROM			22-8550
IC10		74LS377			22-4658
IC11		7533			22-4768
IC12		74LS378			22-4659
IC13		Programmed ROM			22-8551
IC14		74LS378			22-4659
IC15		Programmed ROM			22-8552
IC16		74LS377			22-4658
IC17		74LS378			22-4659
IC18		74LS138			22-4587
Transistors					
Q1		ZTX450			22-6112
Q2		ZTX109			22-6122

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Connectors					
PL39		Connector, 50-way			23-3340
PL40		Connector, 40-way			23-3339

PARTS LIST

FM SYSTEM MODULE 11-1535

Fig 27

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Resistors	Ω		W		
R1	2.7k	Carbon Film	0.1	5	20-1547
R2	100	Carbon Film	0.1	5	20-1514
R3	2k	Variable			20-7093
R4	6.8k	Carbon Film	0.1	5	20-1549
R5	100	Carbon Film	0.1	5	20-1514
R6	4.7k	Carbon Film	0.1	5	20-1542
R7	1.8k	Carbon Film	0.1	5	20-1539
R8	10k	Carbon Film	0.1	5	20-1538
R9	10k	Carbon Film	0.1	5	20-1538
R10	560	Carbon Film	0.1	5	20-1536
R11	2.2k	Carbon Film	0.1	5	20-1528
R12	3.3k	Carbon Film	0.1	5	20-1537
Capacitors	F		V		
C1	100µ	Ceramic	12	-20+80	21-1616
C2	47µ	Electrolytic	16		21-0596
C3	47µ	Electroltyc	16		21-0596
C4	100n	Ceramic	12	-20+80	21-1616
C5	100n	Ceramic	12	-20+80	21-1616
C6	22n	Ceramic	25	-20+80	21-1546
C7	22n	Ceramic	25	-20+80	21-1546
C8	100µ	Electrolytic	6.3	20	21-0774
C9	100µ	Electrolytic	6.3	20	21-0774
C10	47µ	Electrolytic	16		21-0596
C11	100n	Ceramic	12	-20+80	21-1616
C12	47µ	Electrolytic	16		21-0596
Diodes					
D1		Voltage regulator (BZX79C5V6)			22-1809

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Integrated Circuits					
IC1		TL081			22-4229
IC2		74LS138			22-4587
IC3		4042			22-4702
Connectors					
PL56 PL61		Coaxial cable assembly (RC10)			10-2774
PL62		PCB header, 50-way			23-3340
PL63		PCB header, 40-way			23-3339
SK64		Receptacle, coaxial			23-3338
SK65		Receptacle, coaxial			23-3338

PARTS LIST

REFERENCE GENERATOR AND LF SYNTHESIZER MODULE 11-1534

Fig 29

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Resistors	Ω		W		
R1	330	Carbon Film	¼	5	20-2331
R2	10k	Metal Oxide	¼	1	20-4033
R3	8.2k	Metal Oxide	¼	1	20-4013
R4	1.2k	Metal Oxide	¼	1	20-4103
R5	10k	Variable			20-7040
R6	10k	Variable			20-7040
R7	10k	Variable			20-7040
R8	10k	Variable			20-7040
R9	10k	Variable			20-7040
R10	10k	Variable			20-7040
R11	10k	Variable			20-7040
R12	1.1k	Metal Oxide	¼	1	20-4040
R13	1.1k	Metal Oxide	¼	1	20-4040
R14	1.1k	Metal Oxide	¼	1	20-4040
R15	1.1k	Metal Oxide	¼	1	20-4040
R16	1.1k	Metal Oxide	¼	1	20-4040
R17	1.1k	Metal Oxide	¼	1	20-4040
R18	4.7k	Carbon Film	¼	5	20-2472
R19	820	Carbon Film	¼	5	20-2821
R20	4.7k	Carbon Film	0.1	5	20-1542
R21	820	Carbon Film	0.1	5	20-1535
R22	4.7k	Carbon Film	0.1	5	20-1542
R23	820	Carbon Film	0.1	5	20-1535
R24	4.7k	Carbon Film	0.1	5	20-1542
R25	820	Carbon Film	0.1	5	20-1535
R26	4.7k	Carbon Film	0.1	5	20-1542
R27	820	Carbon Film	0.1	5	20-1535
R28	4.7k	Carbon Film	¼	5	20-2472
R29	820	Carbon Film	¼	5	20-2821
R30	10k	Variable			20-7040
R31	10k	Variable			20-7040
R32	10k	Variable			20-7040
R33	10k	Variable			20-7040
R34	10k	Variable			20-7040
R35	10k	Variable			20-7040

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
R36	10k	Variable	¼		20-7040
R37	3.3k	Metal Oxide	¼	1	20-4074
R38	3.3k	Metal Oxide	¼	1	20-4074
R39	3.3k	Metal Oxide	¼	1	20-4074
R40	3.3k	Metal Oxide	¼	1	20-4074
R41	3.3k	Metal Oxide	¼	1	20-4074
R42	3.3k	Metal Oxide	¼	1	20-4074
R116	1k	Carbon Film	0.1	5	20-1521
Capacitors					
	F		V		
C1	47µ	Electrolytic	16		21-0596
C2	100µ	Electrolytic	6.3		21-0774
C3	47µ	Electrolytic	16		21-0596
C4	33µ	Electroltytic	25		21-0782
C5	33µ	Electrolytic	25		21-0782
C6	100µ	Electrolytic	6.3		21-0774
C7	100µ	Electrolytic	6.3		21-0774
C8	100µ	Electrolytic	6.3		21-0774
C9	10n	Ceramic	25	-20+80	21-1545
C10	100n	Ceramic	12	-20+80	21-1616
C11	10n	Ceramic	25	-20+80	21-1545
C12	1n	Ceramic	500	20	21-1532
C13	1n	Ceramic	500	20	21-1532
C14	100n	Ceramic	12	-20+80	21-1616
C15	100n	Ceramic	12	-20+80	21-1616
C16	100n	Ceramic	12	-20+80	21-1616
Diodes					
D1		Silicon (1N4149)			22-1029
D2		Silicon (1N4149)			22-1029
D3		Silicon (1N4149)			22-1029
D4		Silicon (1N4149)			22-1029
D5		Silicon (1N4149)			22-1029
D6		Silicon (1N4149)			22-1029
Transistors					
Q147		ZTX313L			22-6079

Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Integrated Circuits					
IC1		TL082			22-4240
IC2		ZN458B			22-4250
IC3		TL084			22-4243
IC4		TL084			22-4243
IC5		TL084			22-4243
IC6		TL084			22-4243
IC7		TL084			22-4243
IC8		TL082			22-4240
Connectors					
PL41		PCB header, 50-way			23-3340
PL42		PCB header, 40-way			23-3339
SK47		Coaxial receptacle			23-3371
SK48		Coaxial receptacle			23-3371

PARTS LIST

MODULE BLOCK ASSEMBLY

Fig 30

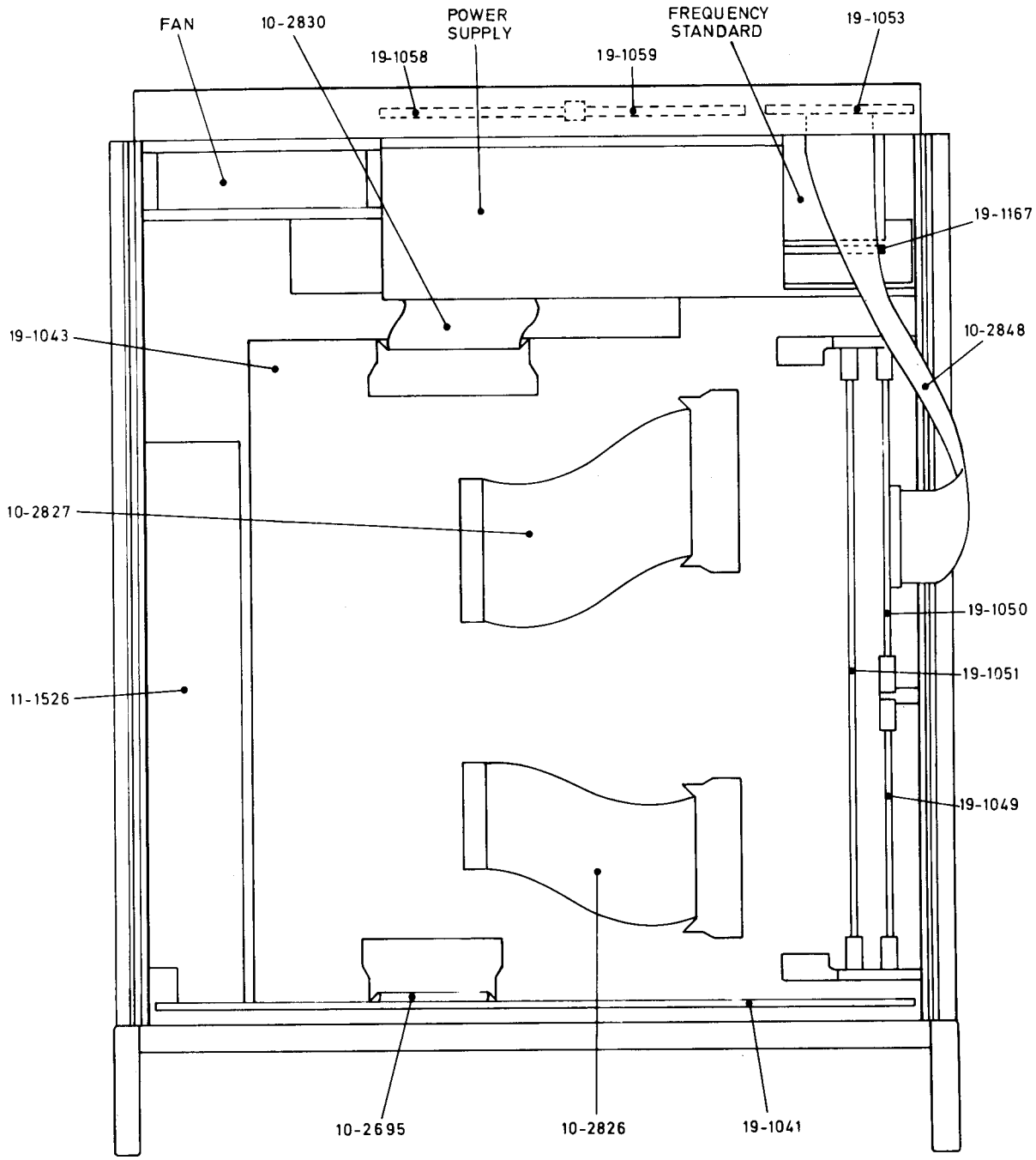
Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Connectors					
RC2		Coaxial cable assembly			10-2776
RC3		Coaxial cable assembly			10-2777
RC4		Coaxial cable assembly			10-2778
RC5		Coaxial cable assembly			10-2779
RC6		Coaxial cable assembly			10-2780
RC7		Coaxial cable assembly			10-2781
RC7		Coaxial cable assembly			10-2782
RC9		Coaxial cable assembly			10-2781
FC0		Coaxial cable assembly			10-2837
FC1		Coaxial cable assembly			10-2833
FC2		Coaxial cable assembly			10-2834
FC3		Coaxial cable assembly			10-2872
FC10		Coaxial cable assembly			10-2873
SK27		Ribbon cable assembly			10-2828
SK26		Ribbon cable assembly			10-2829

PARTS LIST

AUSTRON OSCILLATOR OPTION 19-1158

Fig 31

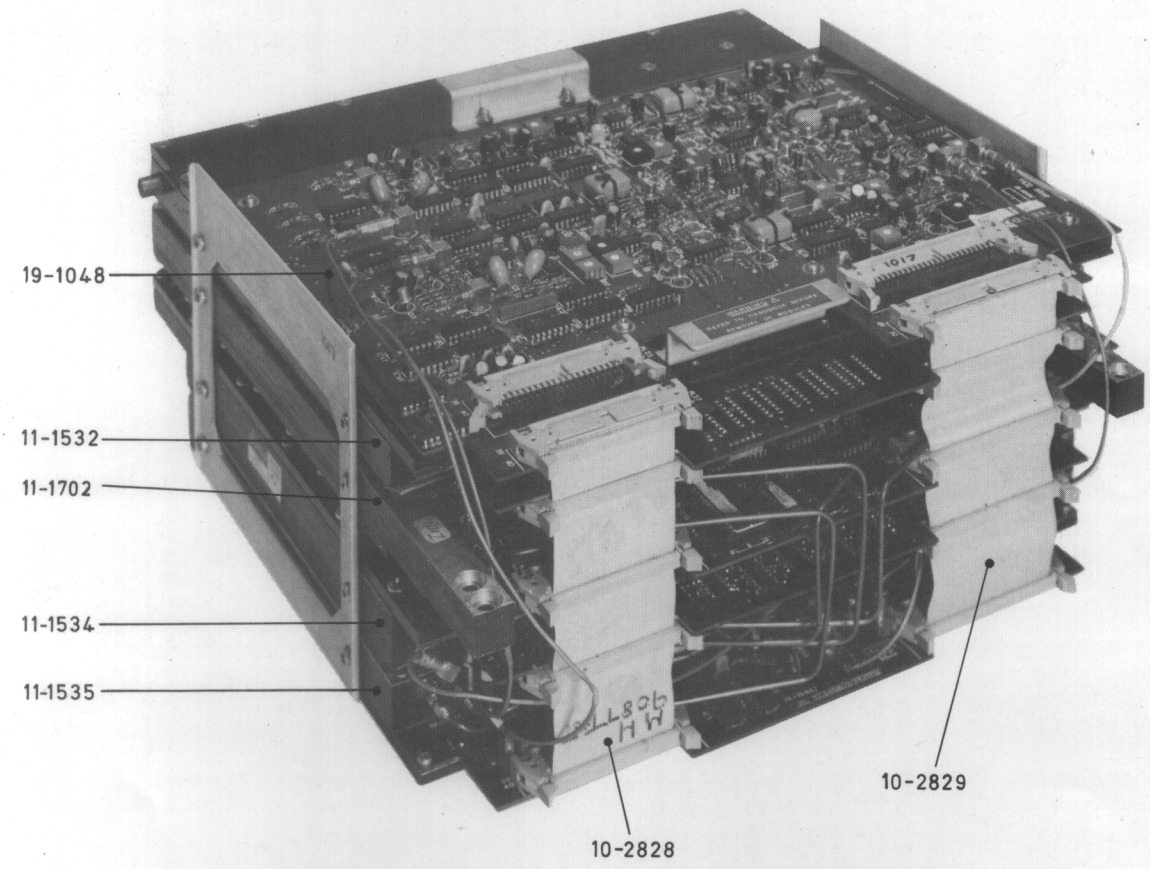
Cct. Ref.	Value	Description	Rat	Tol %	Racal Dana Part Number
Resistors	Ω		W		
R1	15k	Carbon Film	¼	5	20-2153
R2	22k	Carbon Film	¼	5	20-2223
R3	22k	Carbon Film	¼	5	20-2223
R4	1.5k	Metal Oxide	½	5	20-3152
Transistors					
Q1		2N4124			22-6009
Q2		BDT92			22-6153
Q3		ZTX450			22-6112



RACAL
TH3635

Chassis Layout

Fig.1

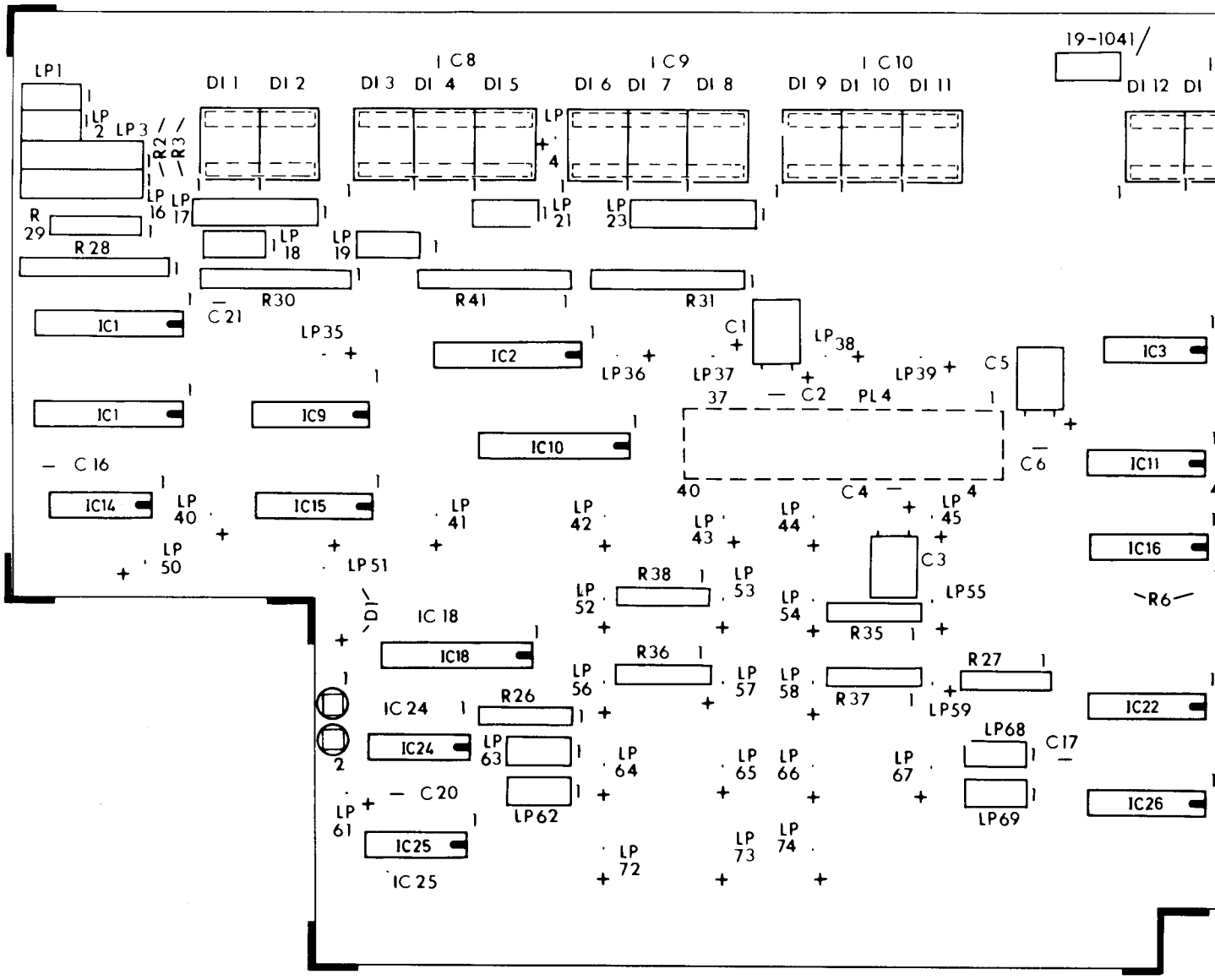


RACAL

TH 3635	11-1531
1	

Module Block Assembly

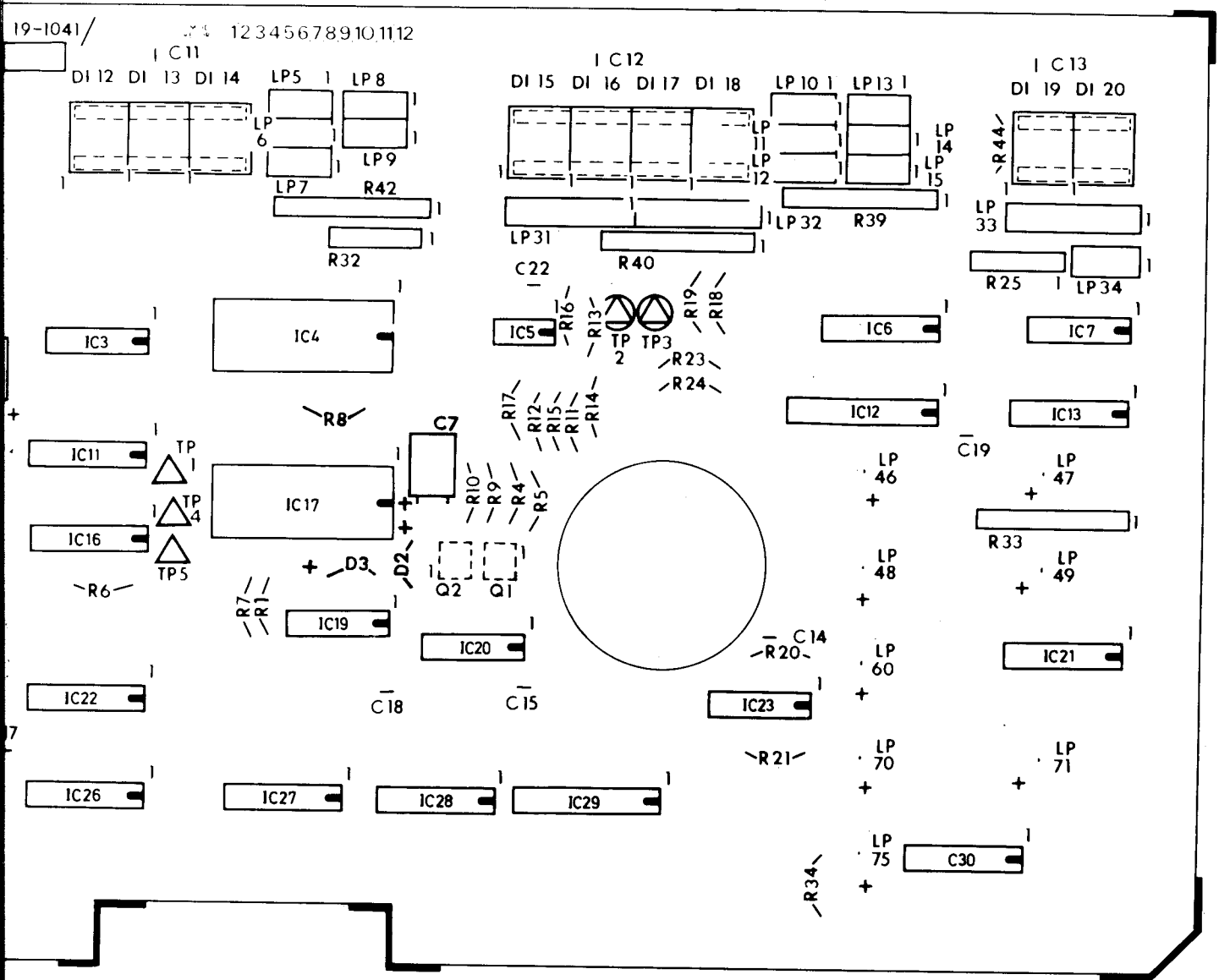
Fig.2



RACAL

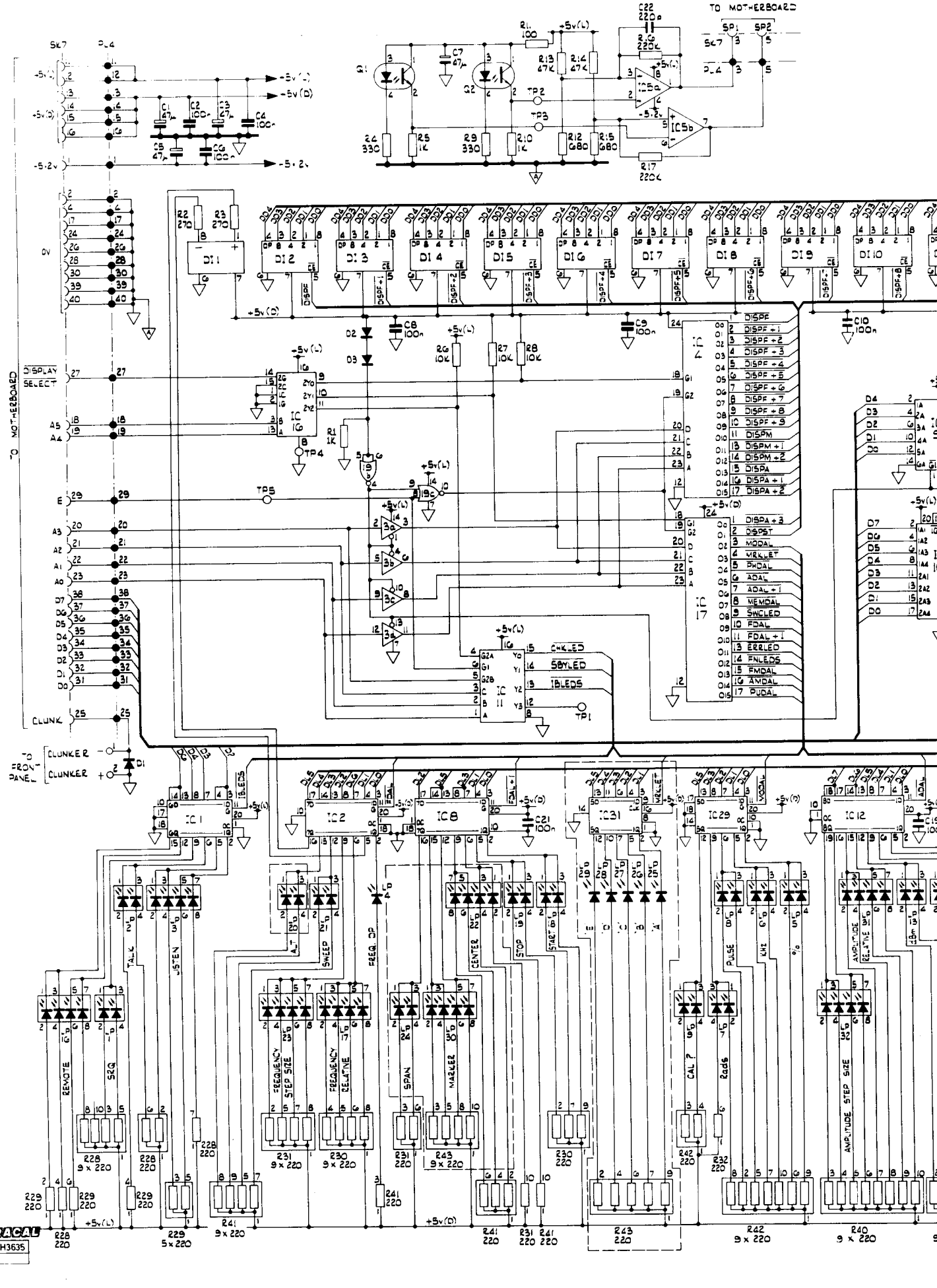
TH3635

2

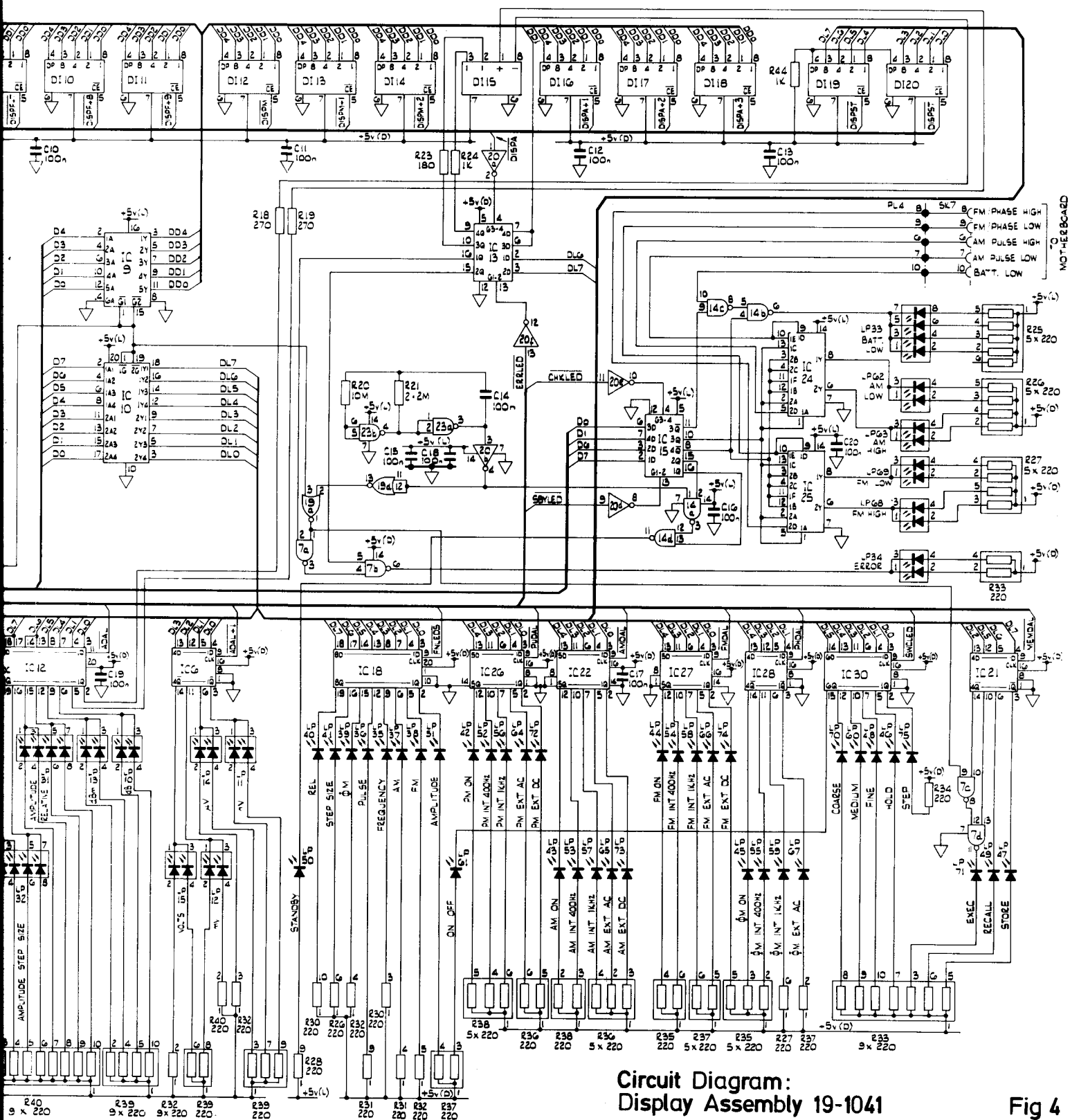


Component Layout :
Display Assembly 19-1041.

Fig 3.

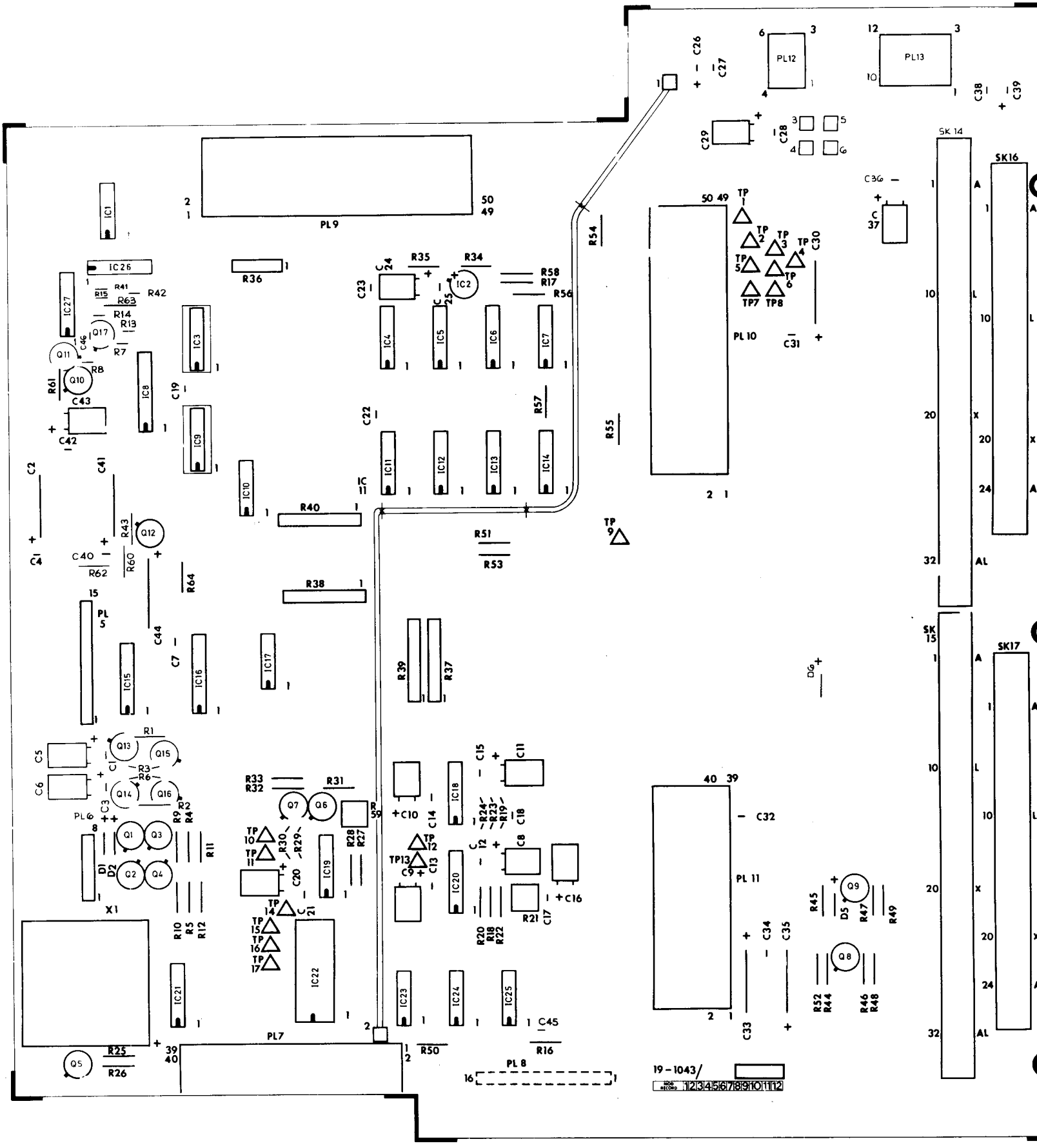

TO MOTHERBOARD
SK7
PL4
-5v(L)
-5v(D)
+5v(L)
+5v(D)
0V
C1 47µ
C2 100n
C3 47µ
C4 100n
C5 47µ
C6 100n
C7 47µ
C8 100n
C9 100n
C10 100n
C21 100n
C22 220p
R1 100
R2 270
R3 270
R4 330
R5 1K
R6 10K
R7 10K
R8 10K
R9 330
R10 1K
R11 220K
R12 680
R13 47K
R14 47K
R15 680
R16 220K
R17 220K
Q1
Q2
TP1
TP2
TP3
TP4
TP5
IC5a
IC5b
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DI8
DI9
DI10
IC 16
IC 17
IC 11
DISPLAY SELECT
CLUNK
TO FRONT PANEL
CLUNKER -
CLUNKER +
D1
D2
D3
IC1
IC2
IC8
IC31
IC29
IC12
LED
REMOTE
SEQ
TALK
LISTEN
FREQUENCY STEP SIZE
FREQUENCY RELATIVE
SWEEP
FREQ. OP
SPAN
MARKER
CENTER
START
STOP
PULSE
kHz
%
CAL ?
Rads
AMPLITUDE RELATIVE
AMPLITUDE STEP SIZE
RACAL
TH3635
2

NOTE
R43, IC31, LP20, 22, 24-30 ARE
NOT FITTED ON THIS ASSY.

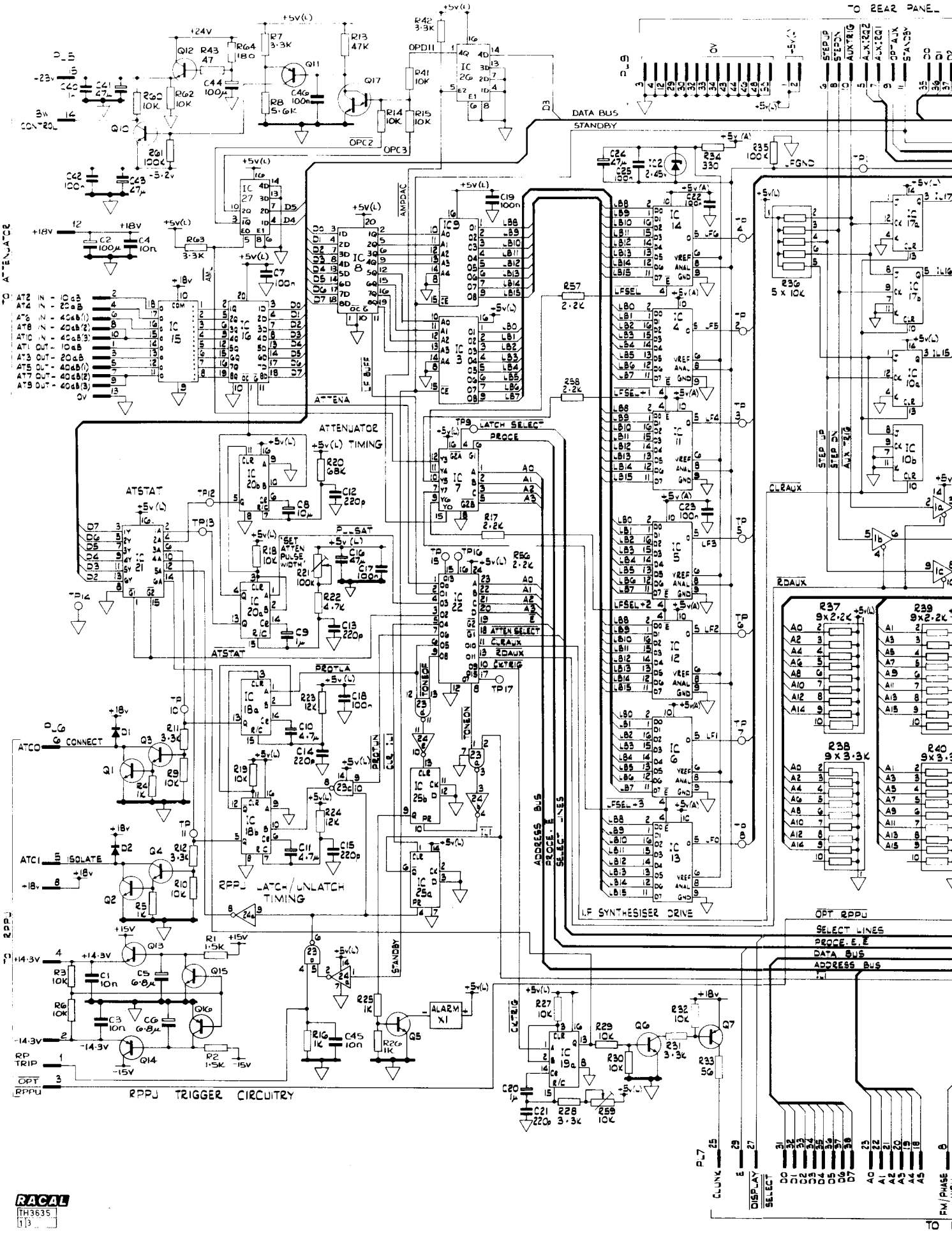


Circuit Diagram:
Display Assembly 19-1041

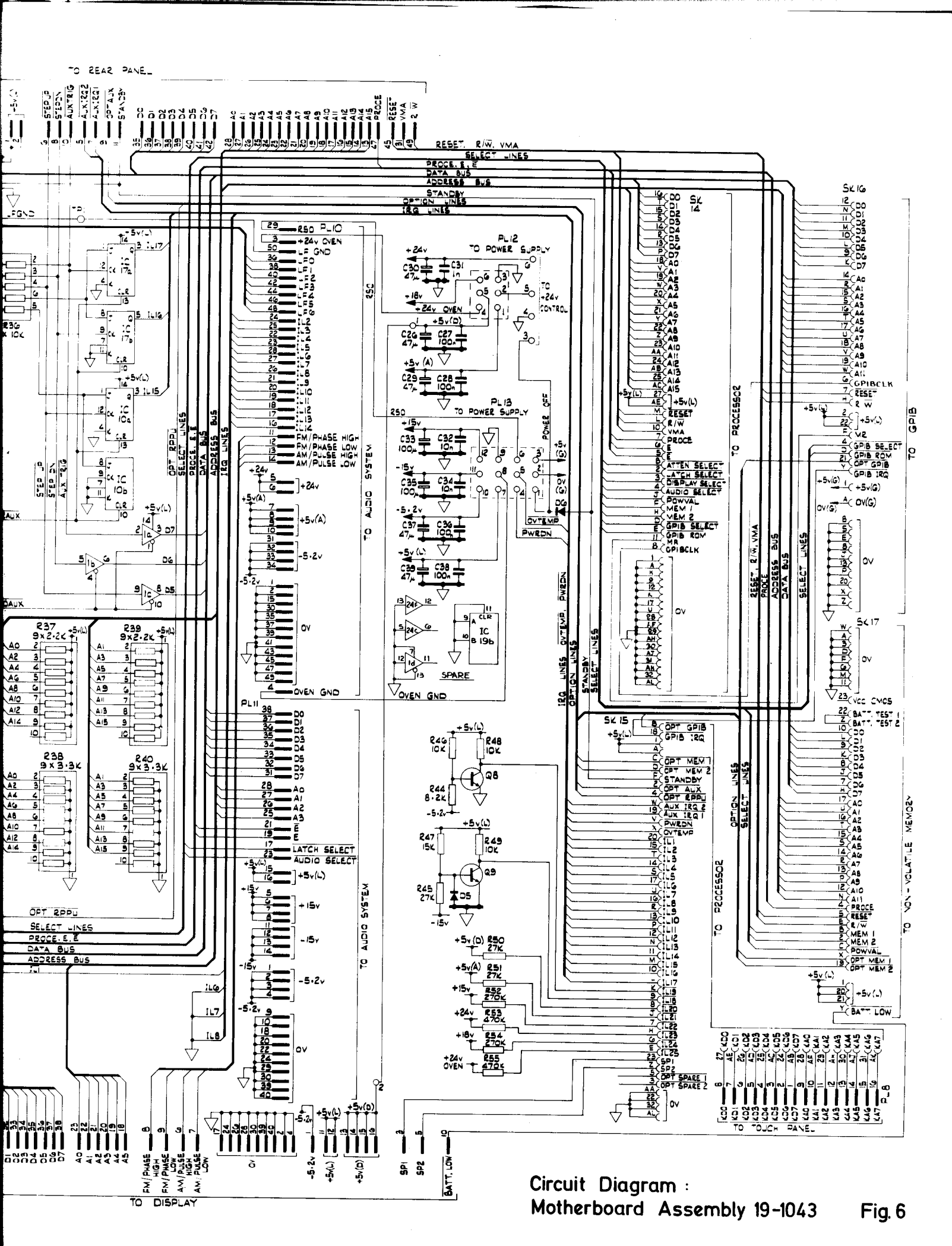
Fig 4



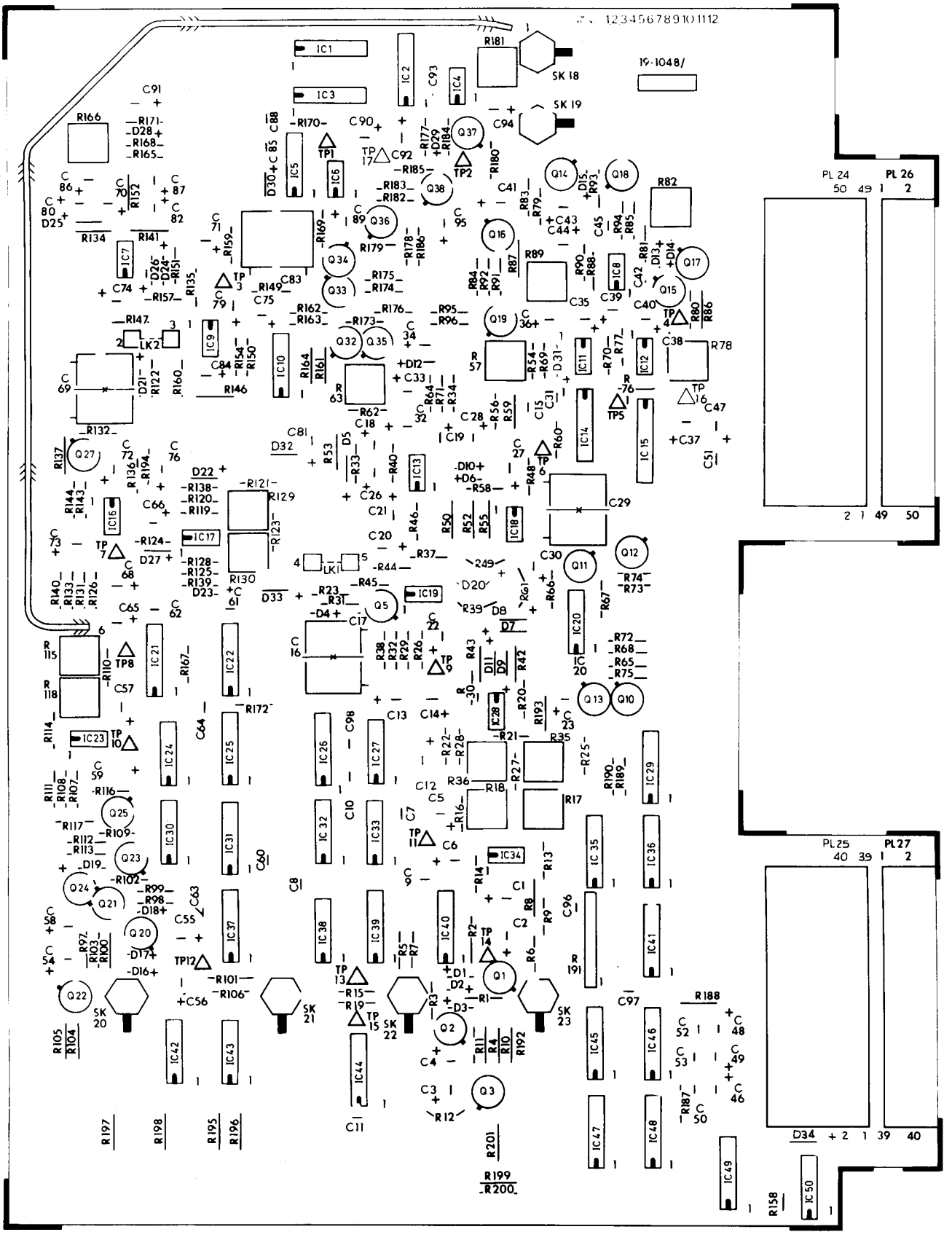
Component Layout :
Motherboard Assembly 19-1043 Fig



RACAL
TH3635
1 3



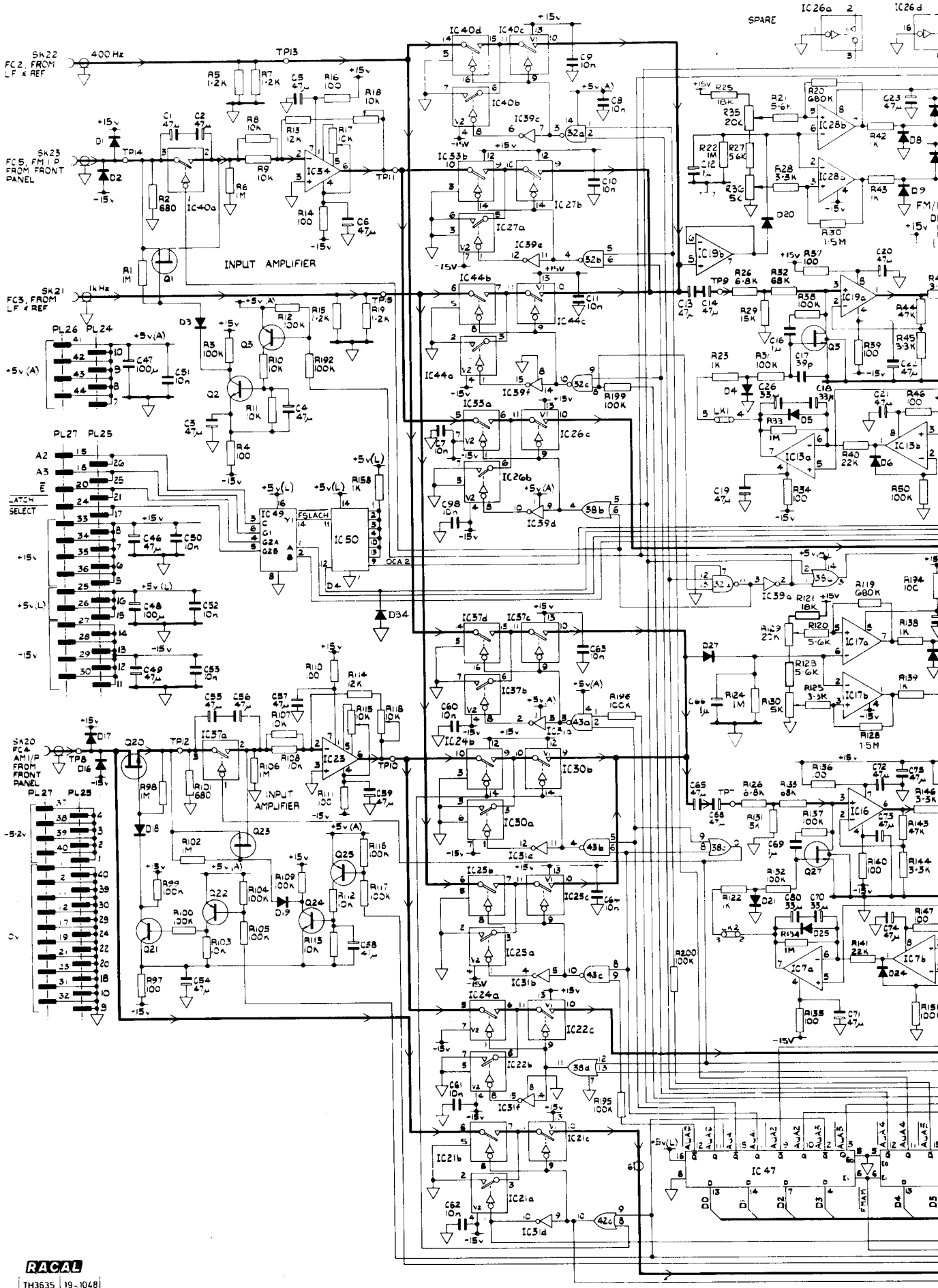
Circuit Diagram :
Motherboard Assembly 19-1043 Fig. 6

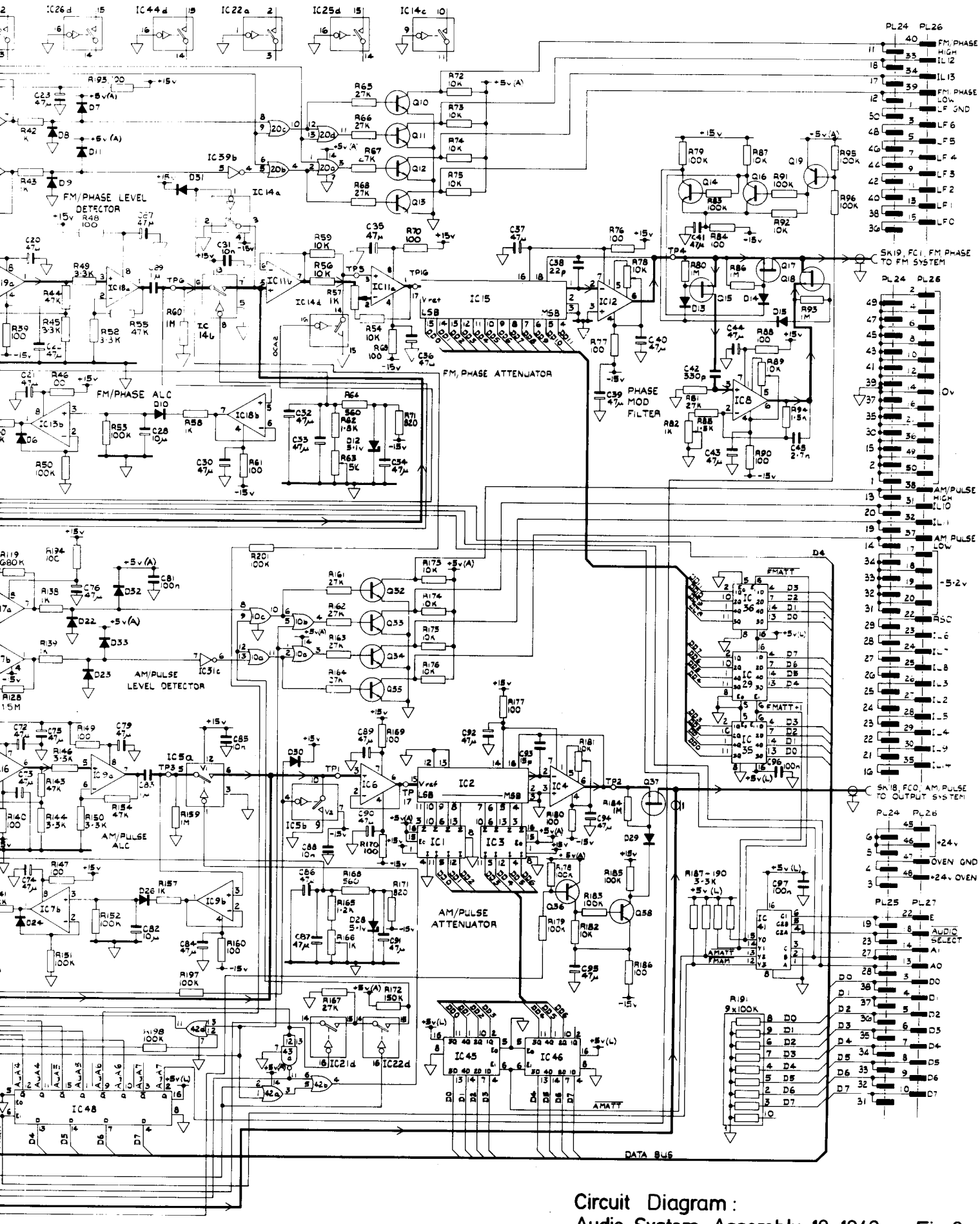


RACAL
TH3635 | 19-1048
3

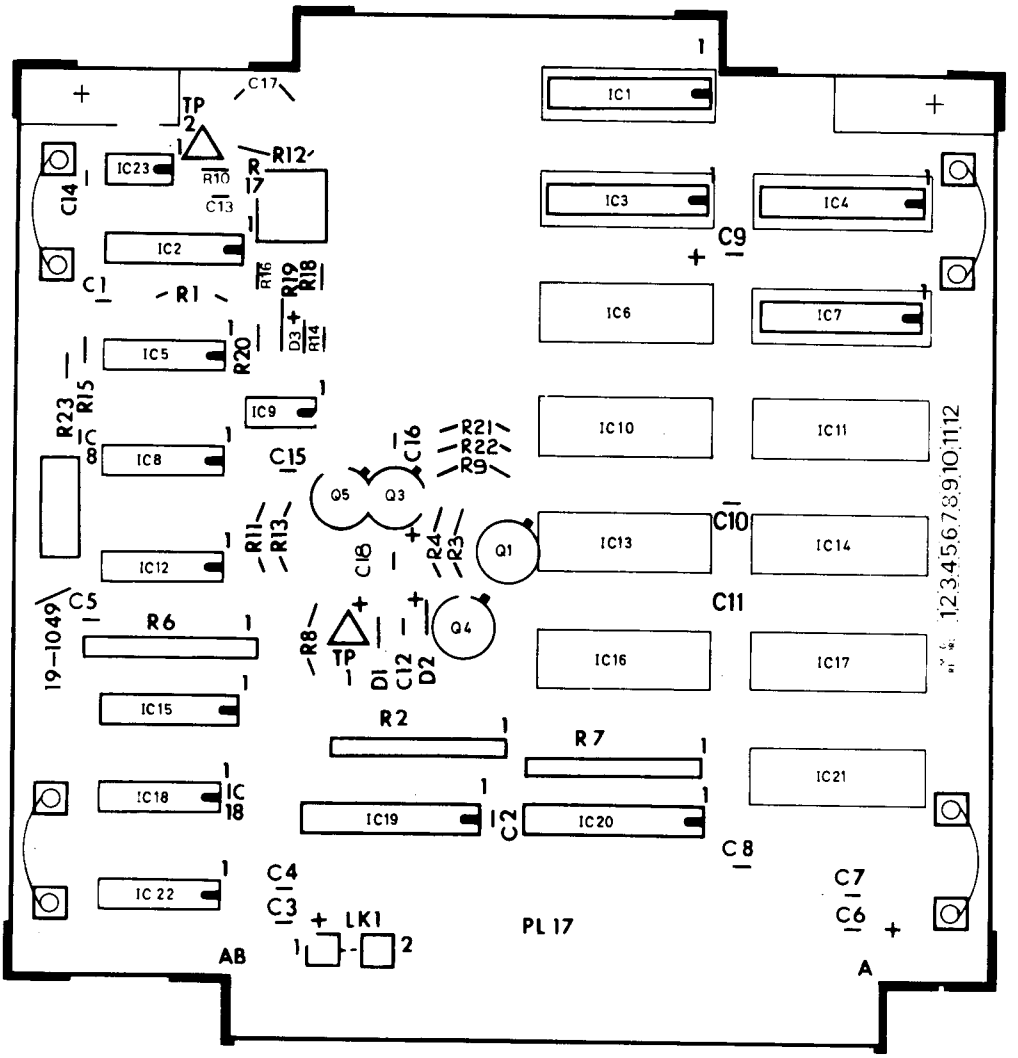
Component Layout :
Audio System Assembly 19-1048

Fig. 7


SK22
FC2, FROM LF & REF
400 Hz
TP13
SK23
FC5, FM I P FROM FRONT PANEL
TP14
TP11
INPUT AMPLIFIER
SK21
FC3, FROM LF & REF
1k Hz
TP5
PL26 PL24
PL27 PL25
LATCH SELECT
FSLACH
IC 50
IC 49
OCA 2
SK20
FC4 AM I/P FROM FRONT PANEL
TP8
TP12
TP10
INPUT AMPLIFIER
PL27 PL25
IC 47
SPARE
IC26a
IC26d
TP9
TP7
LK1
RACAL
TH3635
19-1048
2
3



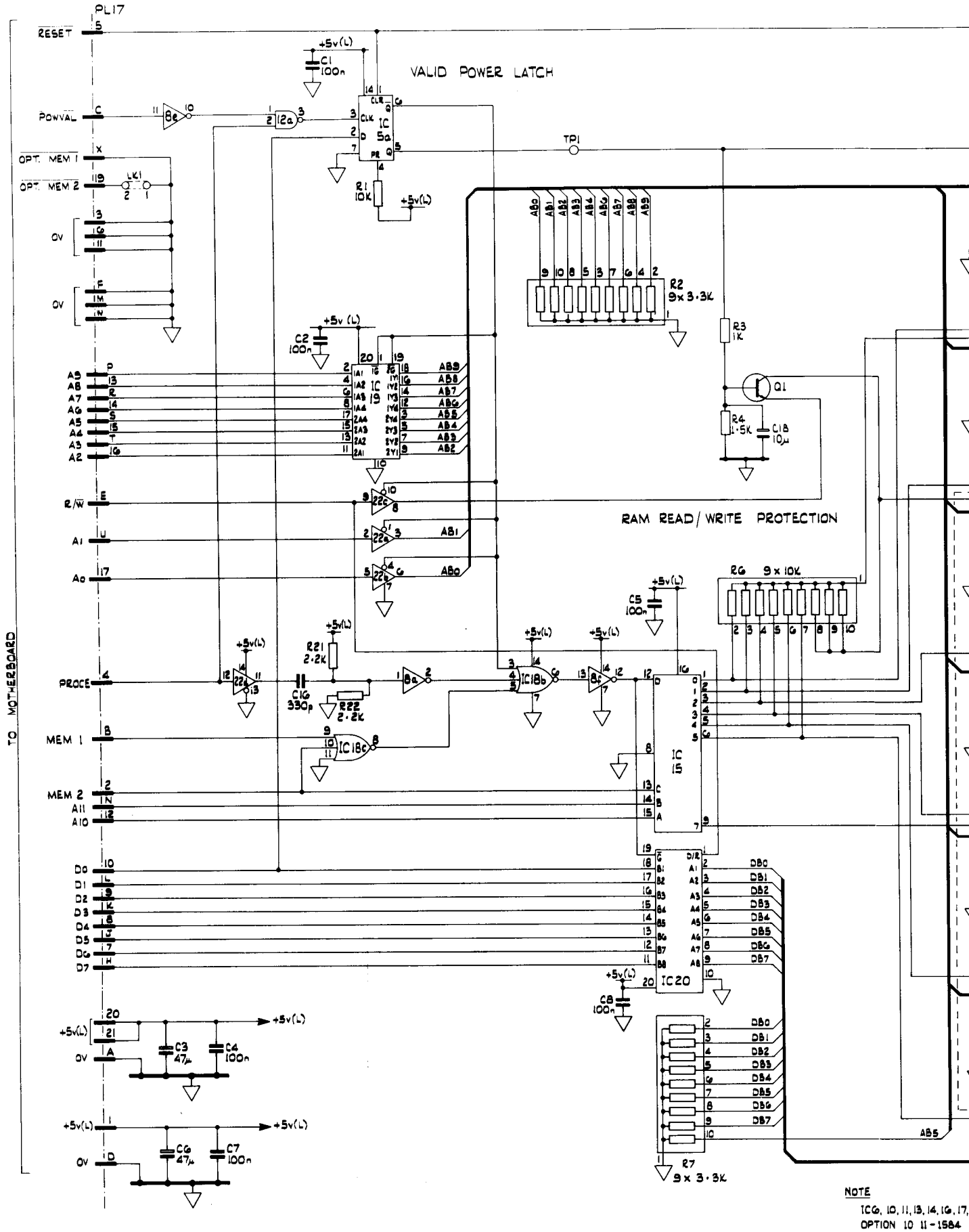
Circuit Diagram :
Audio System Assembly 19-1048. Fig 8.



RACAL
TH3635 19-1049
2

Component Layout:
Non-Volatile Memory Assembly 19-1049

Fig. 9

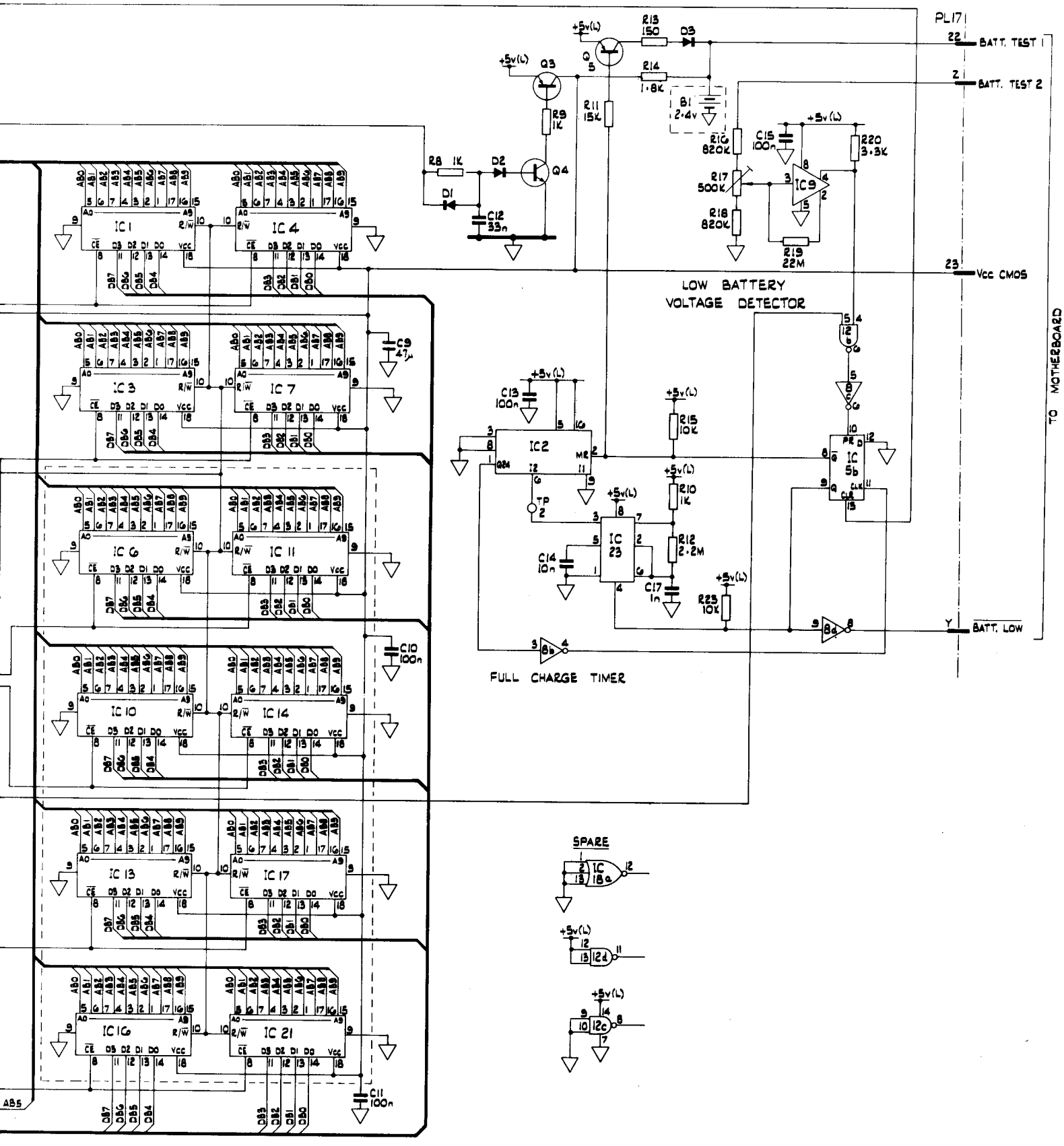


NOTE

ICG, 10, 11, 13, 14, 16, 17,
OPTION 10 11 - 1584

RACAL

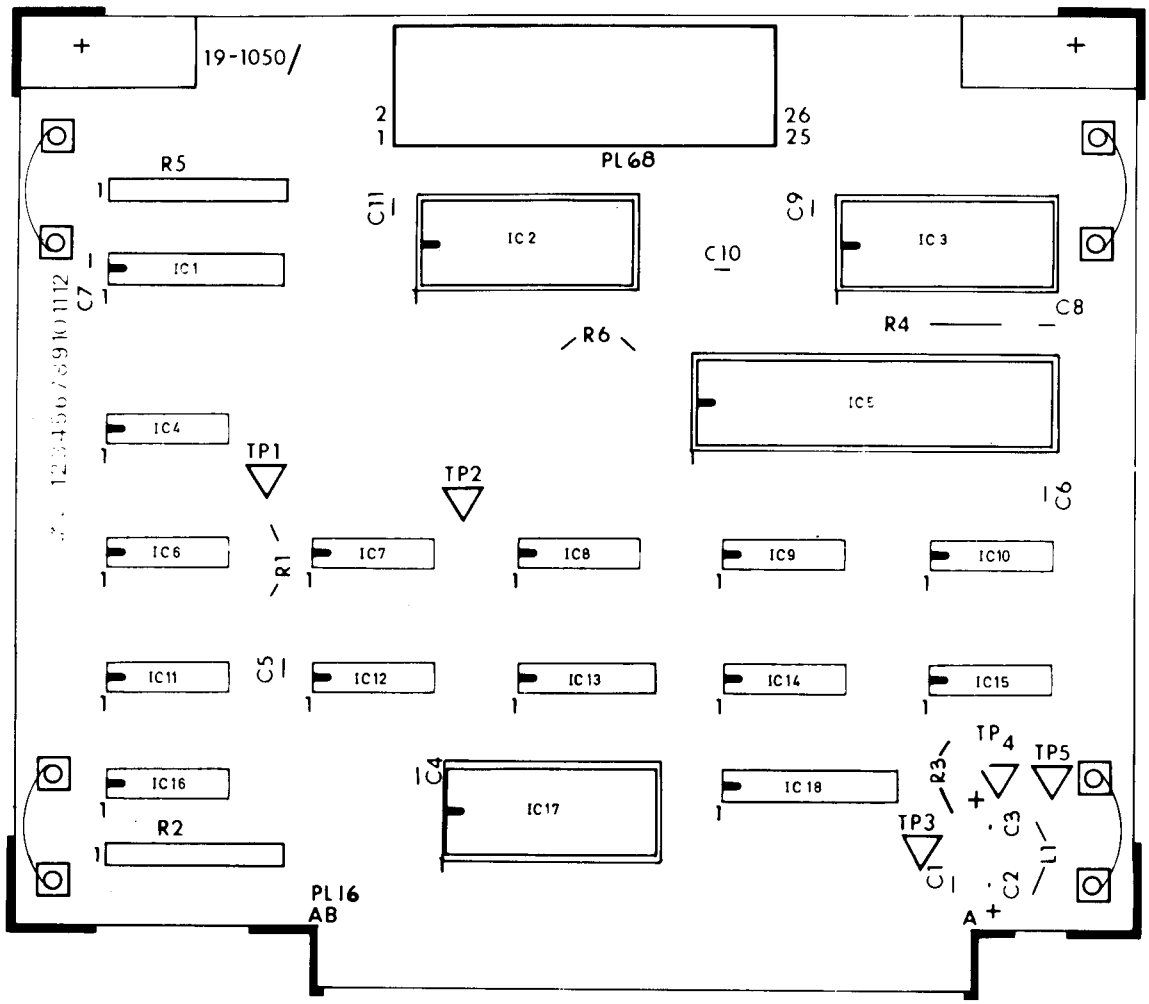
TH3635	19-1049
2	



8, 14, 16, 17, 21 AND LK1 ARE TO BE FITTED FOR
11-1584 MEMORY (100 STORE) OPTION.

Circuit Diagram: Non-Volatile Memory Assembly 19-1049

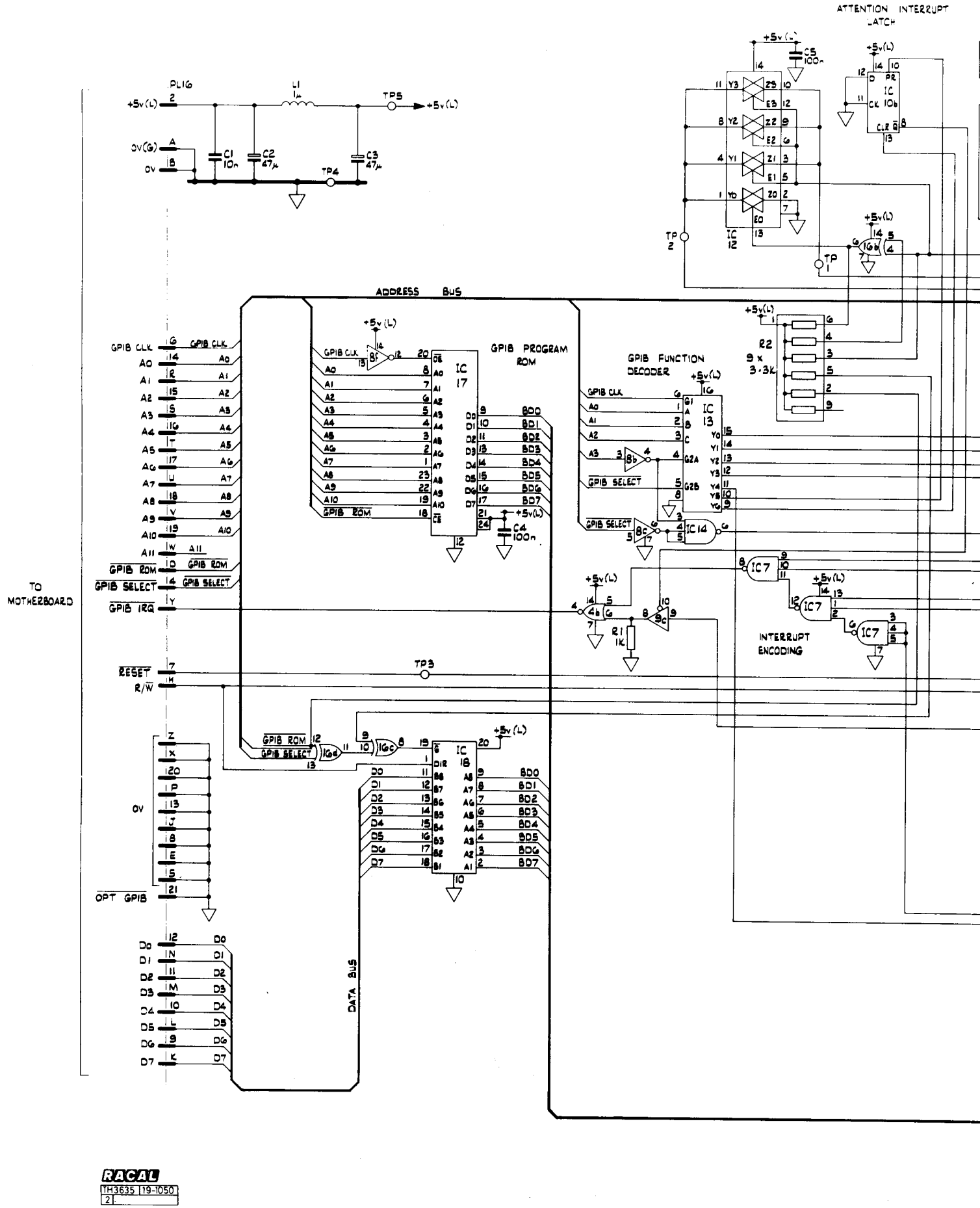
Fig.10



RACAL
TH3635 19-1050
2

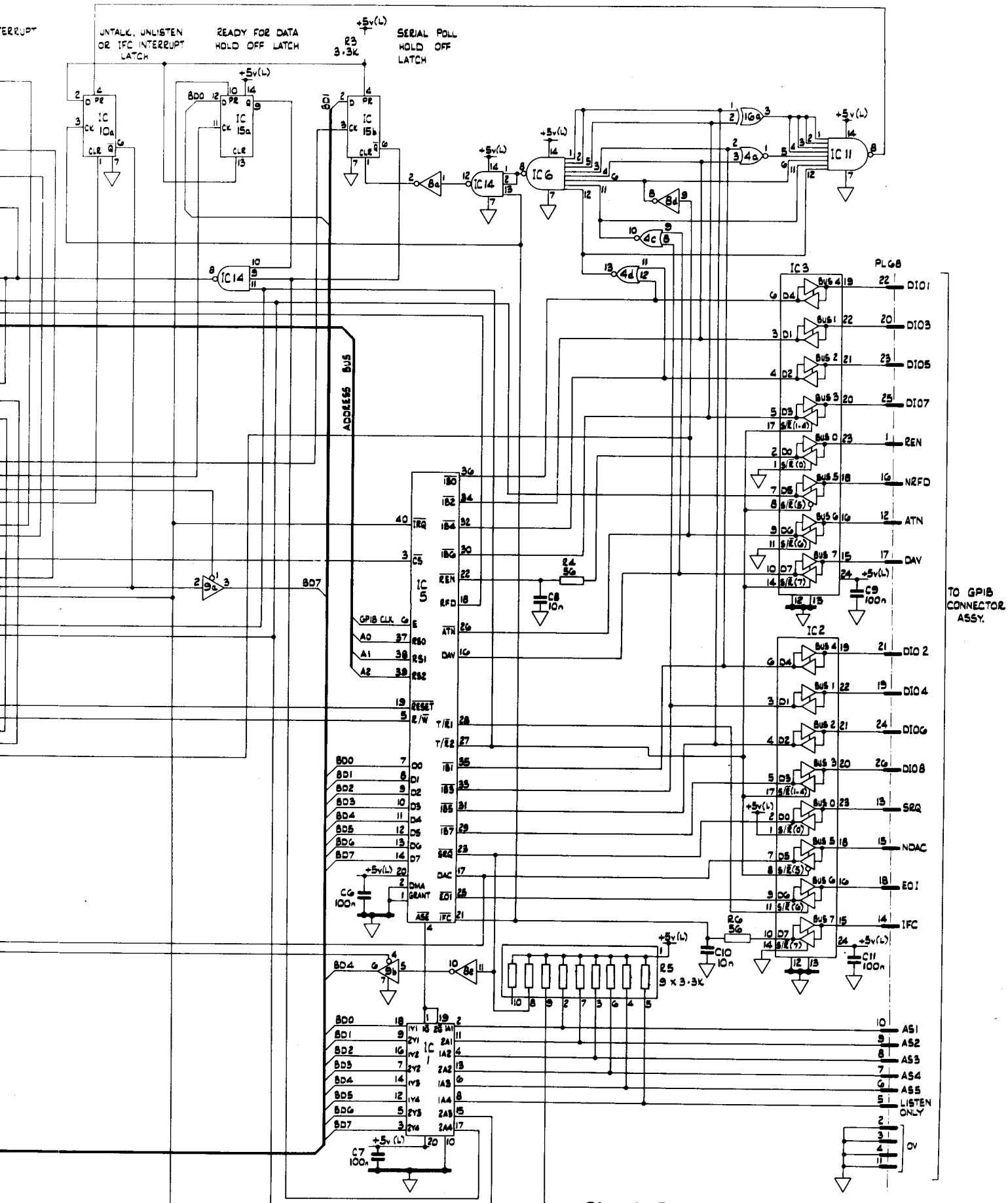
Circuit Diagram :
G.P.I.B Assembly 19-1050

Fig.11



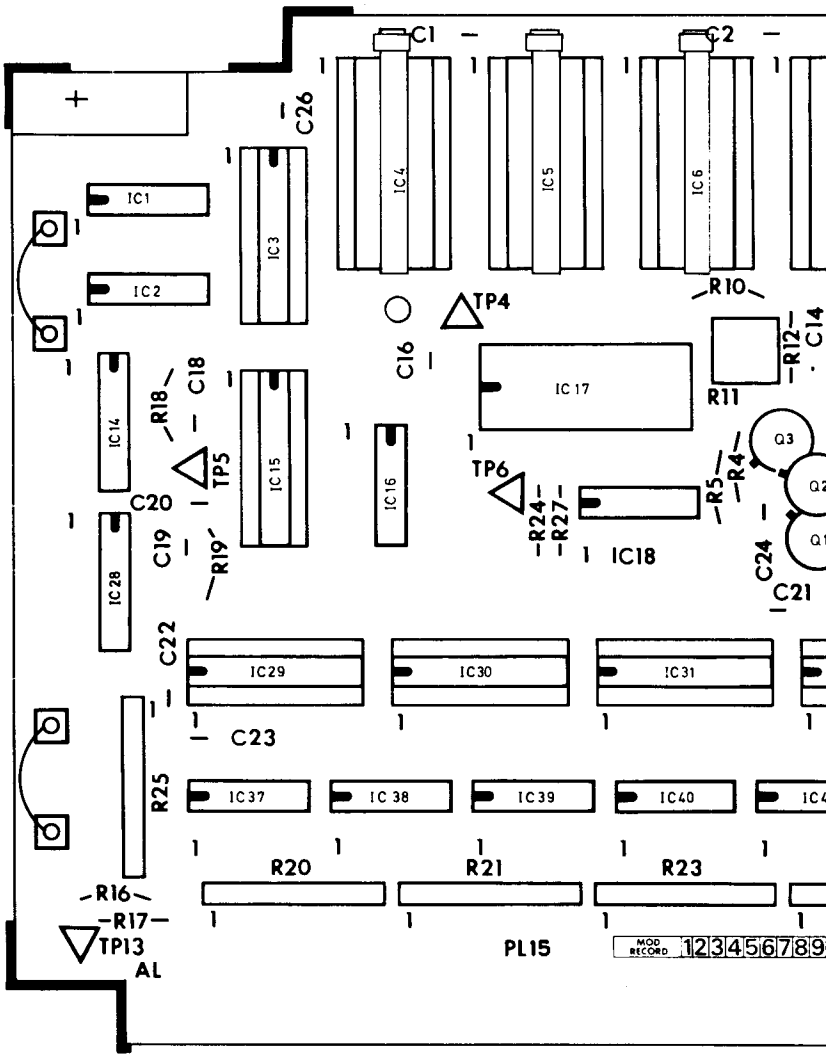
RACAL

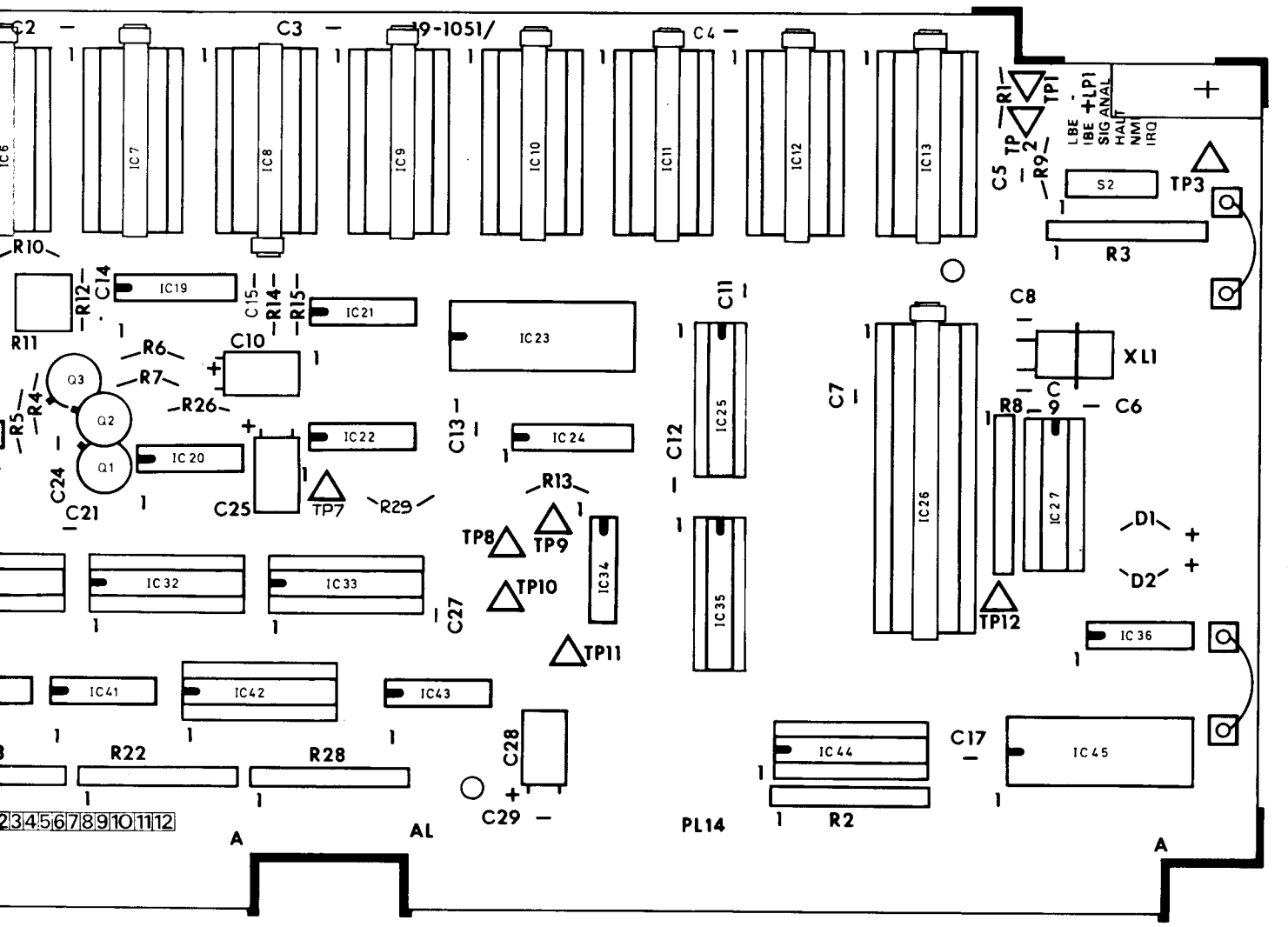
TH3635 [19-1050] [2]



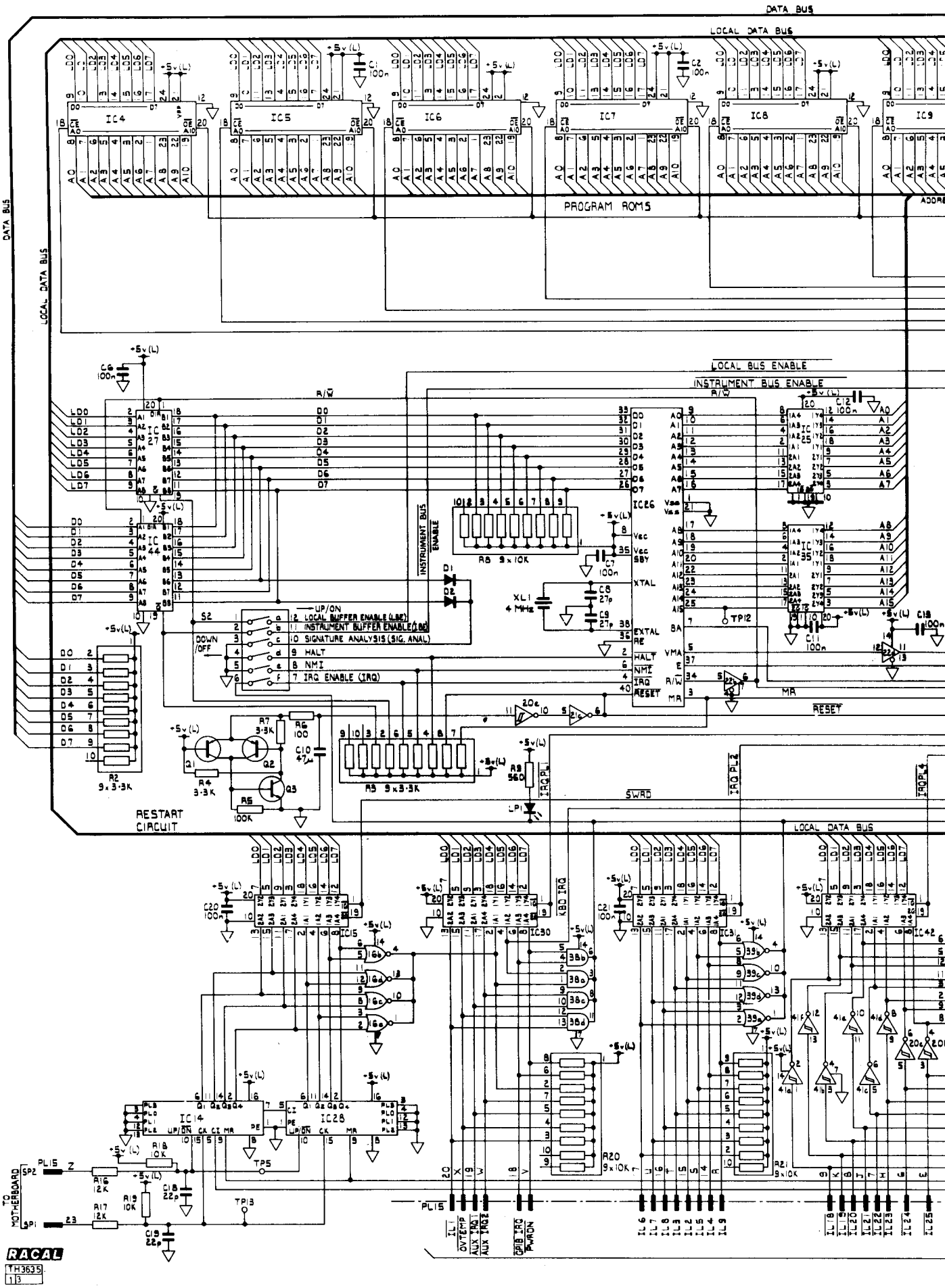
Circuit Diagram:
G.P.I.P Assembly 19-1050

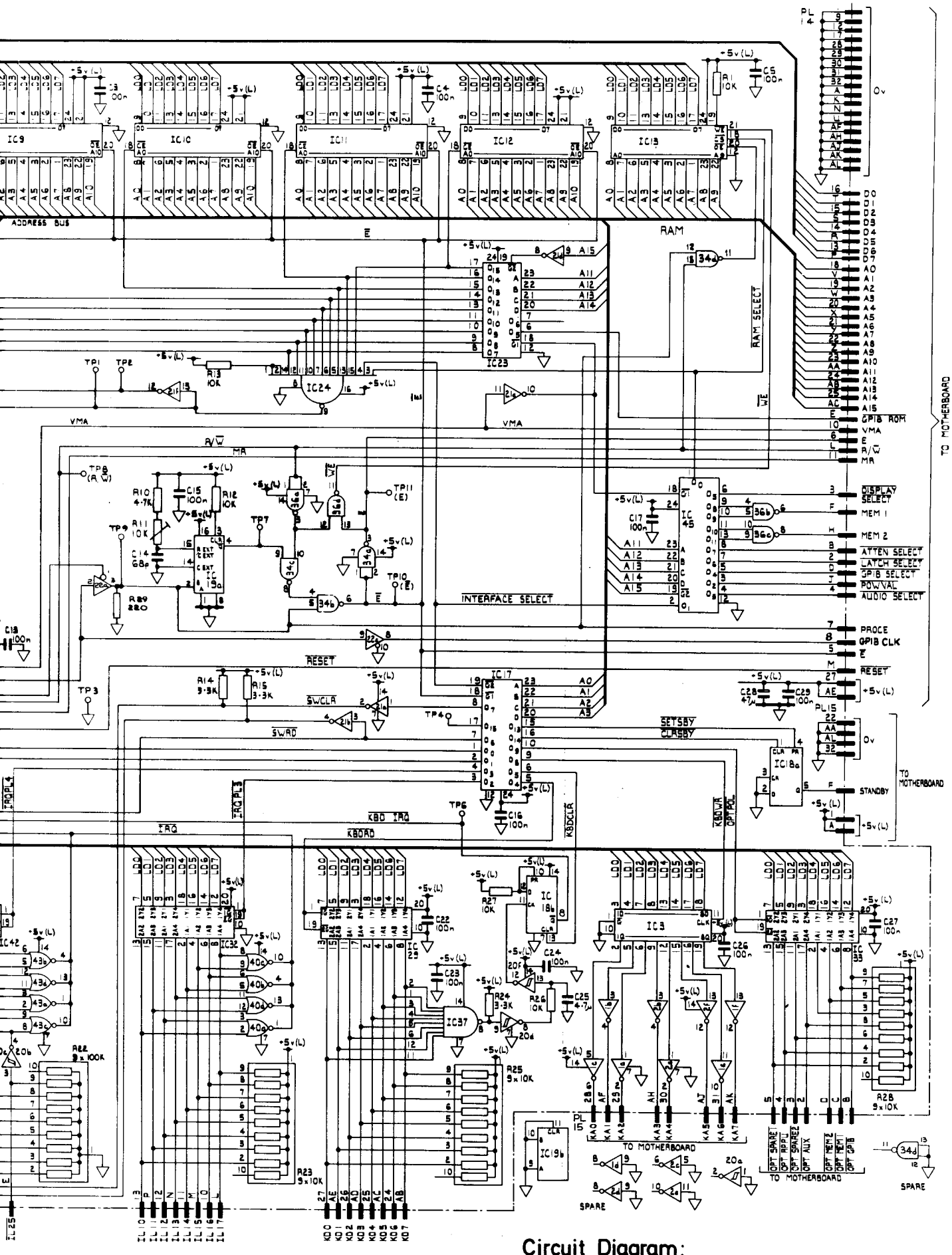
Fig.12


C1
C2
C26
IC1
IC2
IC3
IC4
IC5
IC6
TP4
R10
C16
C18
R18
IC14
IC15
IC16
IC17
R11
R12
C14
TP5
TP6
R4
R5
Q3
C20
C19
R19
IC28
R24
R27
IC18
C24
C21
C22
IC29
IC30
IC31
C23
R25
IC37
IC38
IC39
IC40
R20
R21
R23
R16
R17
TP13
AL
PL15
MOD RECORD 1 2 3 4 5 6 7 8 9



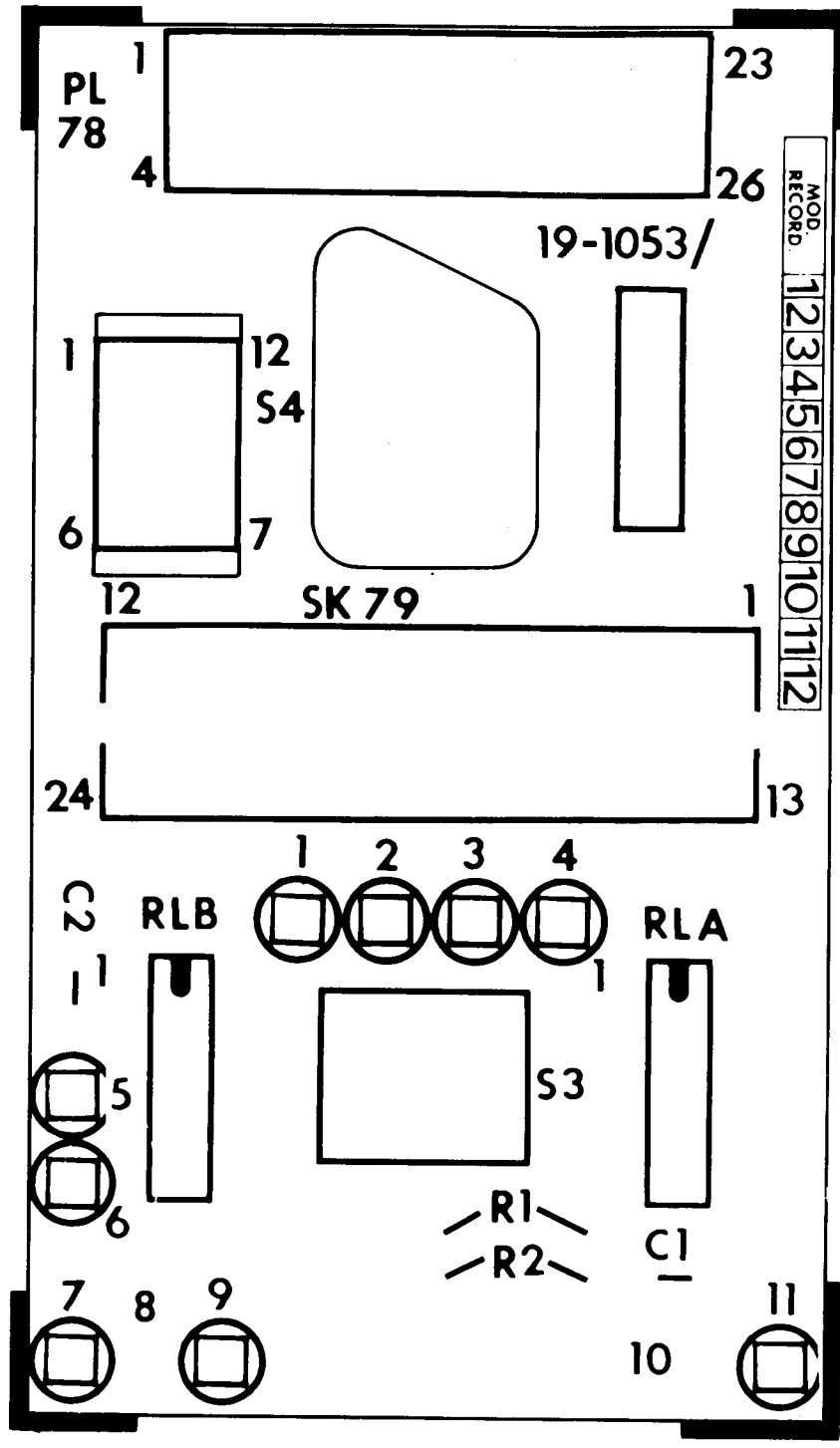
Component Layout:
Processor Assembly 19-1051 Fig.13


DATA BUS
LOCAL DATA BUS
PROGRAM ROMS
LOCAL BUS ENABLE
INSTRUMENT BUS ENABLE
R/W
INSTRUMENT BUS ENABLE
S2
UP/ON
DOWN /OFF
1 LOCAL BUFFER ENABLE (LBE)
2 INSTRUMENT BUFFER ENABLE (IBE)
3 SIGNATURE ANALYSIS (SIG. ANAL)
4 HALT
5 NMI
6 IRQ ENABLE (IRQ)
RESTART CIRCUIT
RESET
SWRD
IRQ PL2
IRQ PL4
KBD IRQ
TO MOTHERBOARD
RACAL
TH3635
1/3



Circuit Diagram:
Processor Assembly 19-1051

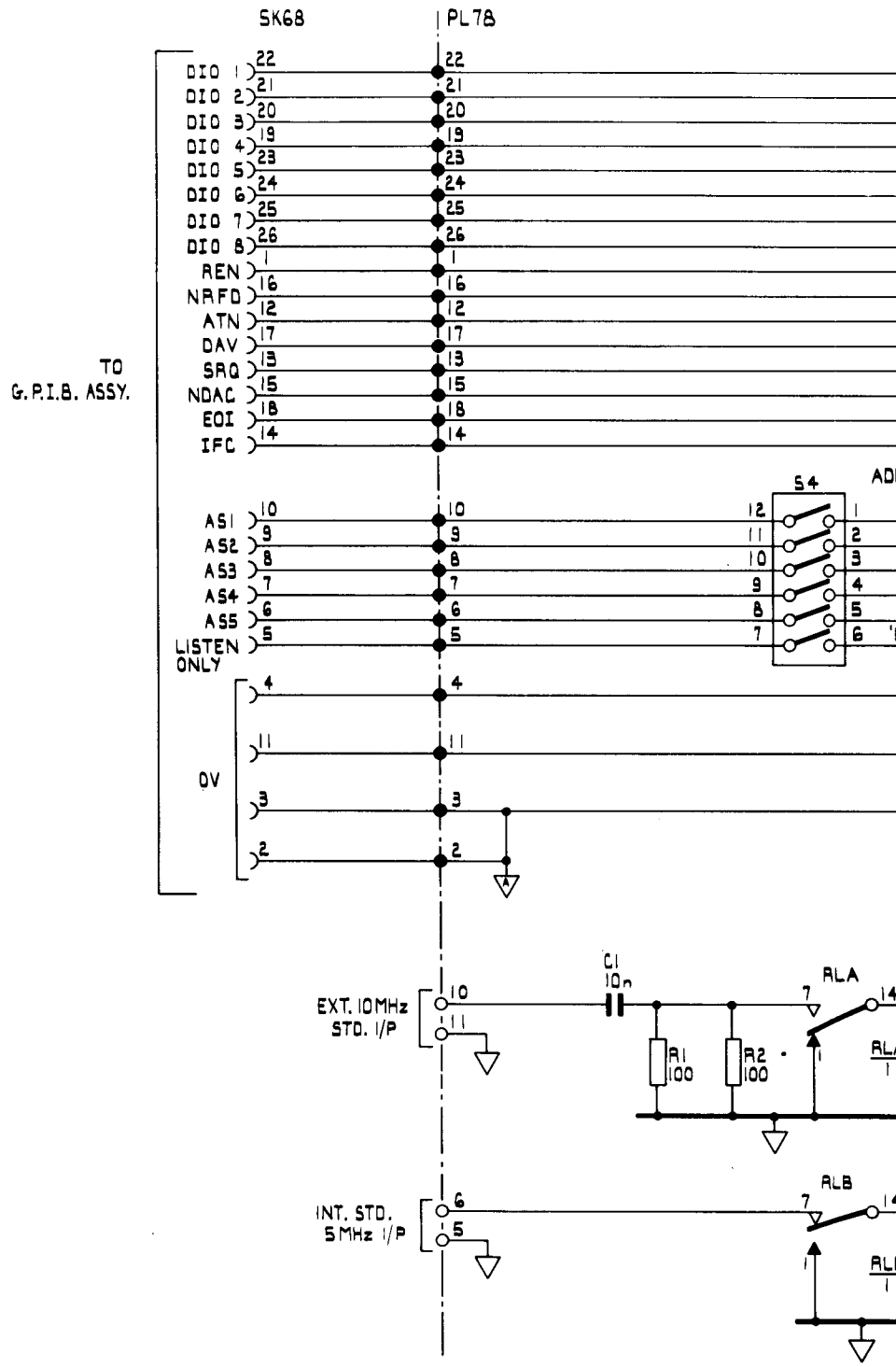
Fig.14

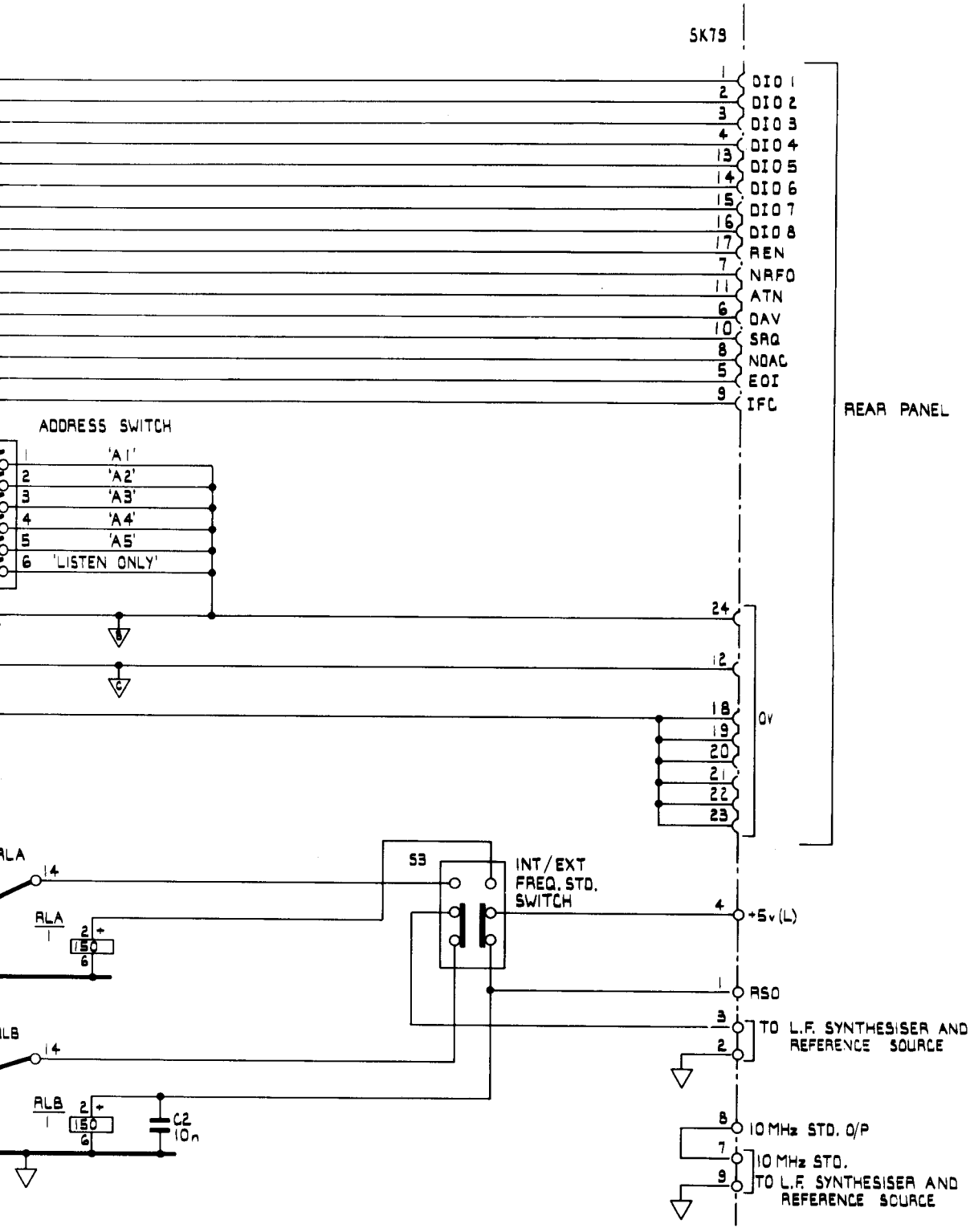


RACAL
TH3635

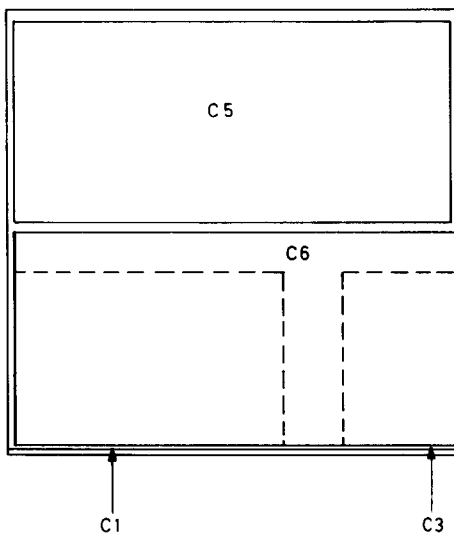
Component Layout : GPIB
Connector Assembly 19-1053.

Fig.15


SK68
PL78
TO
G.P.I.B. ASSY.
DIO 1
DIO 2
DIO 3
DIO 4
DIO 5
DIO 6
DIO 7
DIO 8
REN
NRFD
ATN
DAV
SRQ
NDAC
EOI
IFC
AS1
AS2
AS3
AS4
AS5
LISTEN ONLY
0V
S4
EXT. 10MHz STD. I/P
INT. STD. 5MHz I/P
C1 10n
R1 100
R2 100
RLA
RLB



Circuit Diagram : GPIB Connector Assembly 19-1053. Fig.16.



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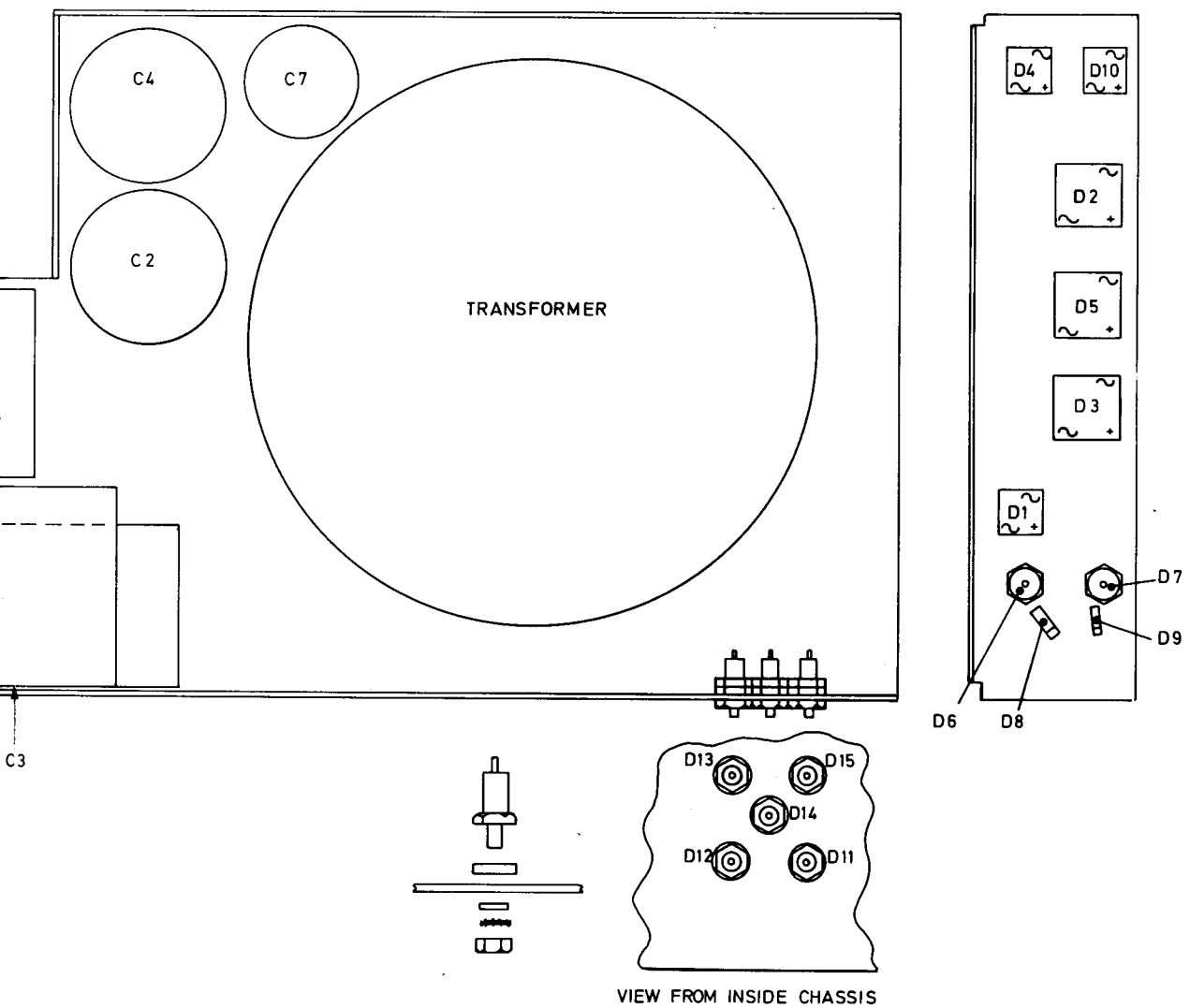
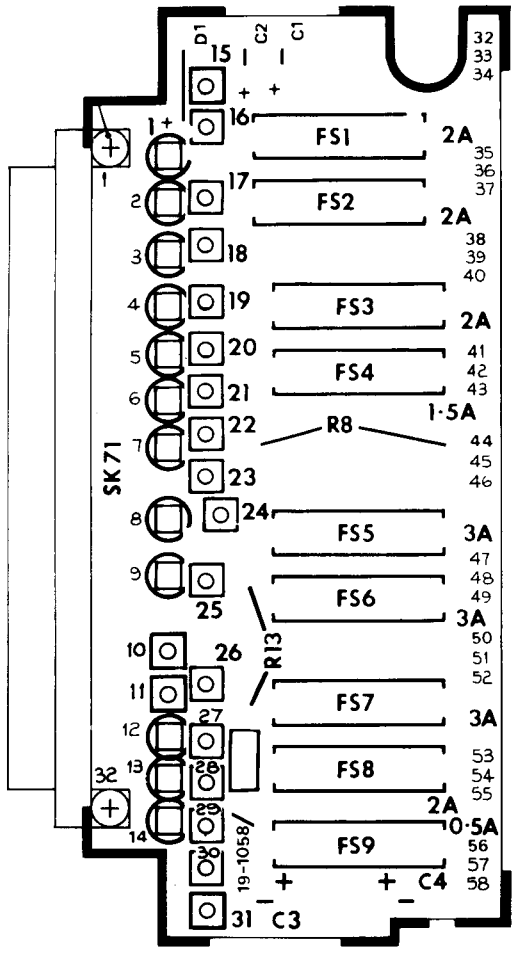
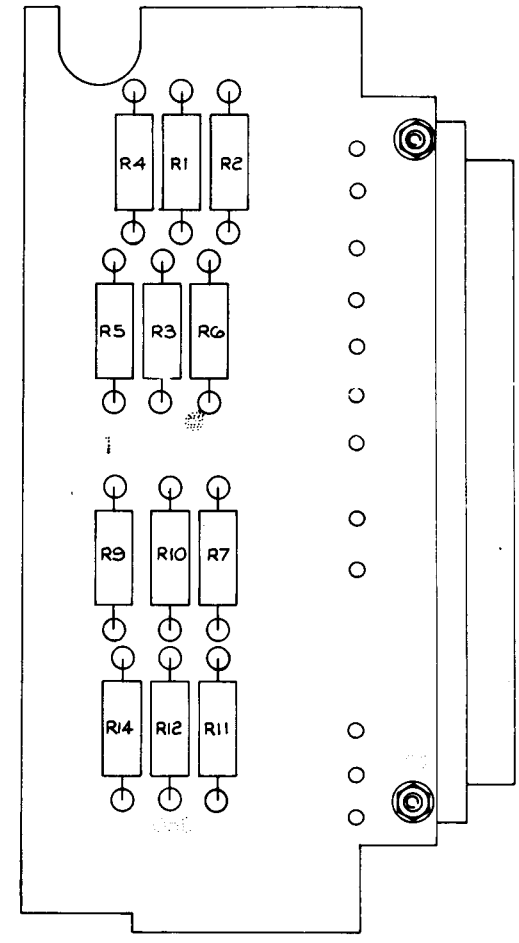


Power Supply Chassis Layout Fig.17



COMP. SIDE



TRACKSIDE

Component Layout
Power Supply Interconnect Assembly
19-1058

Fig.18

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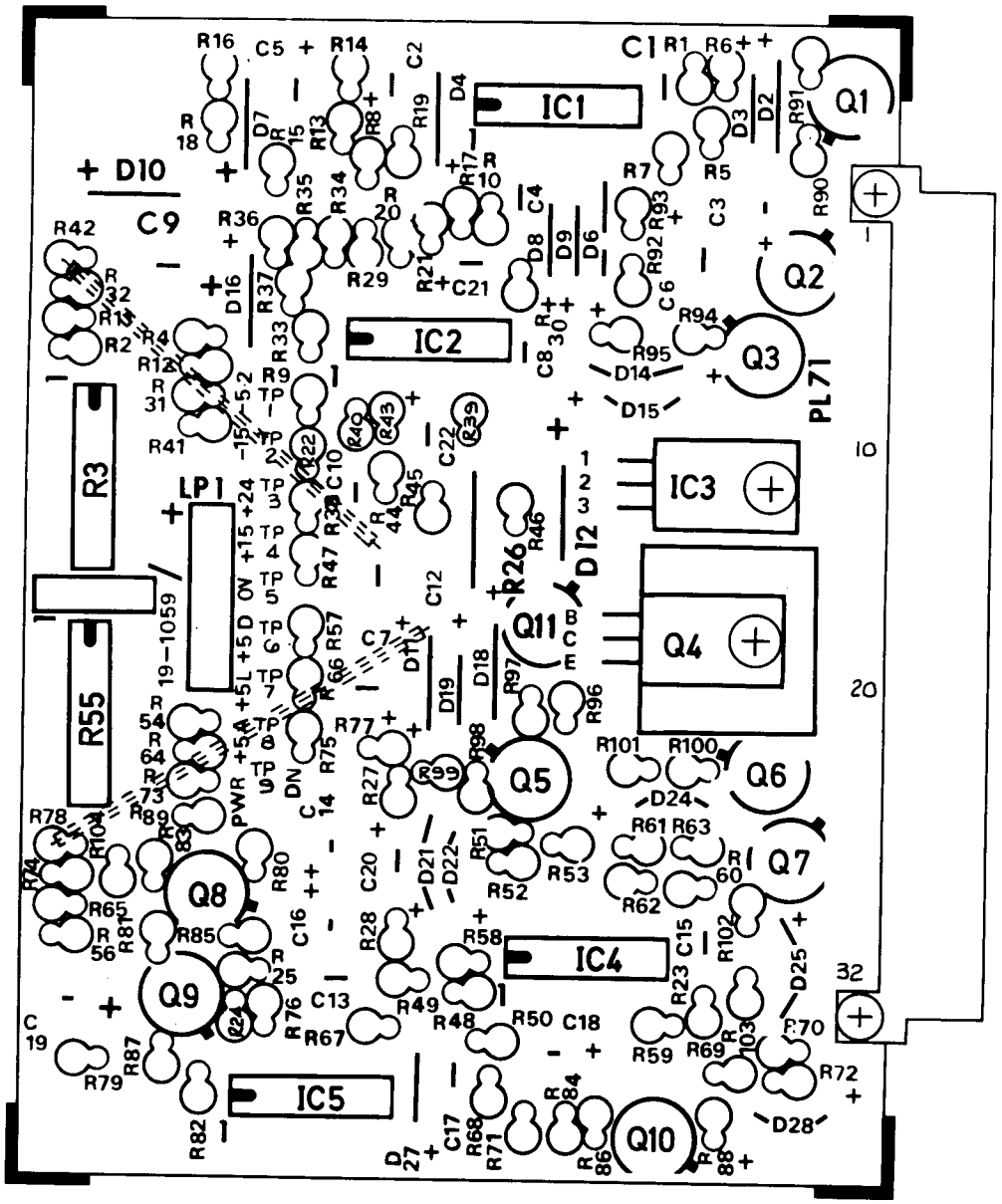
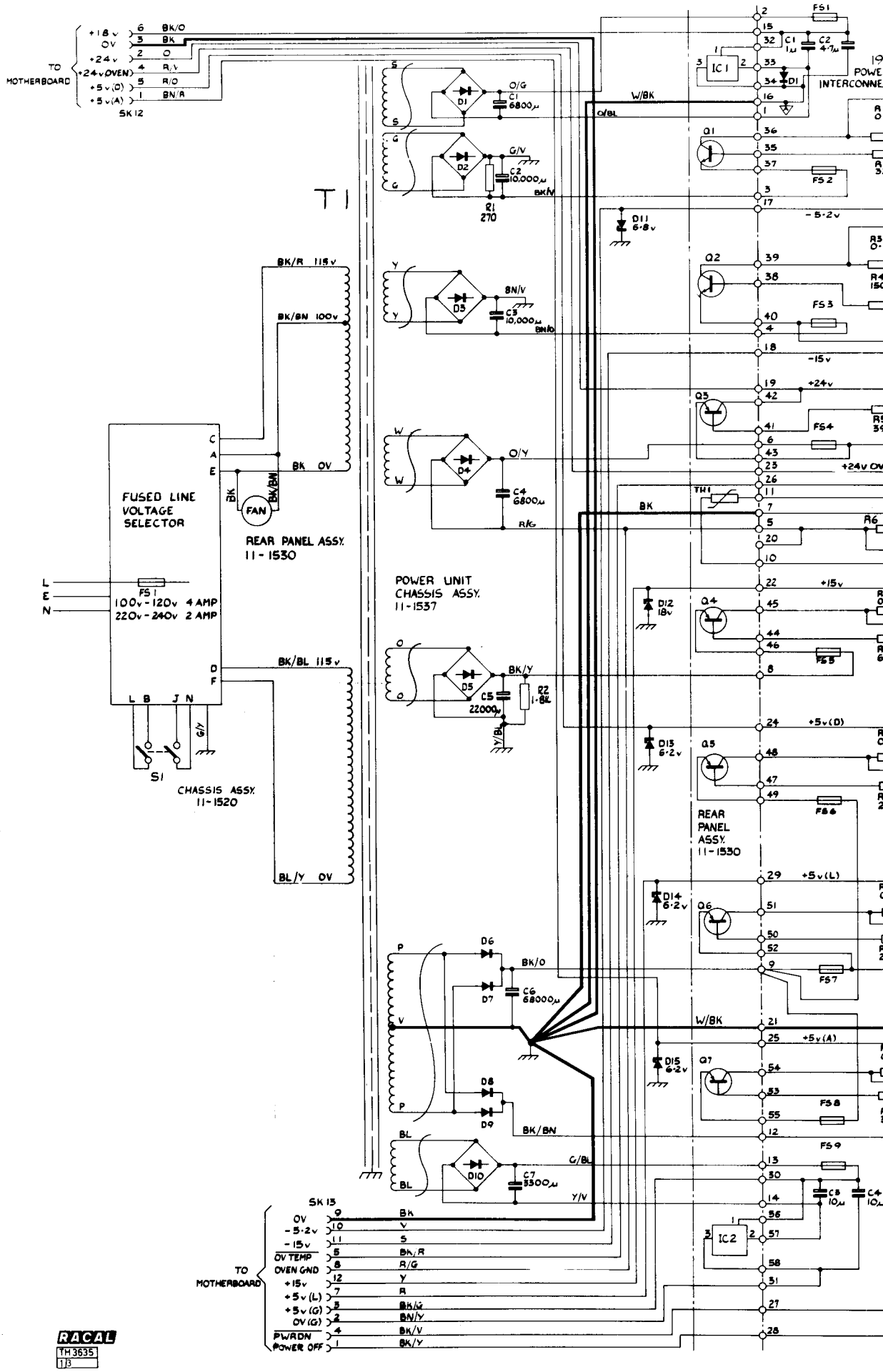


Component Layout :
Power Supply Control Assembly 19-1059. Fig.19



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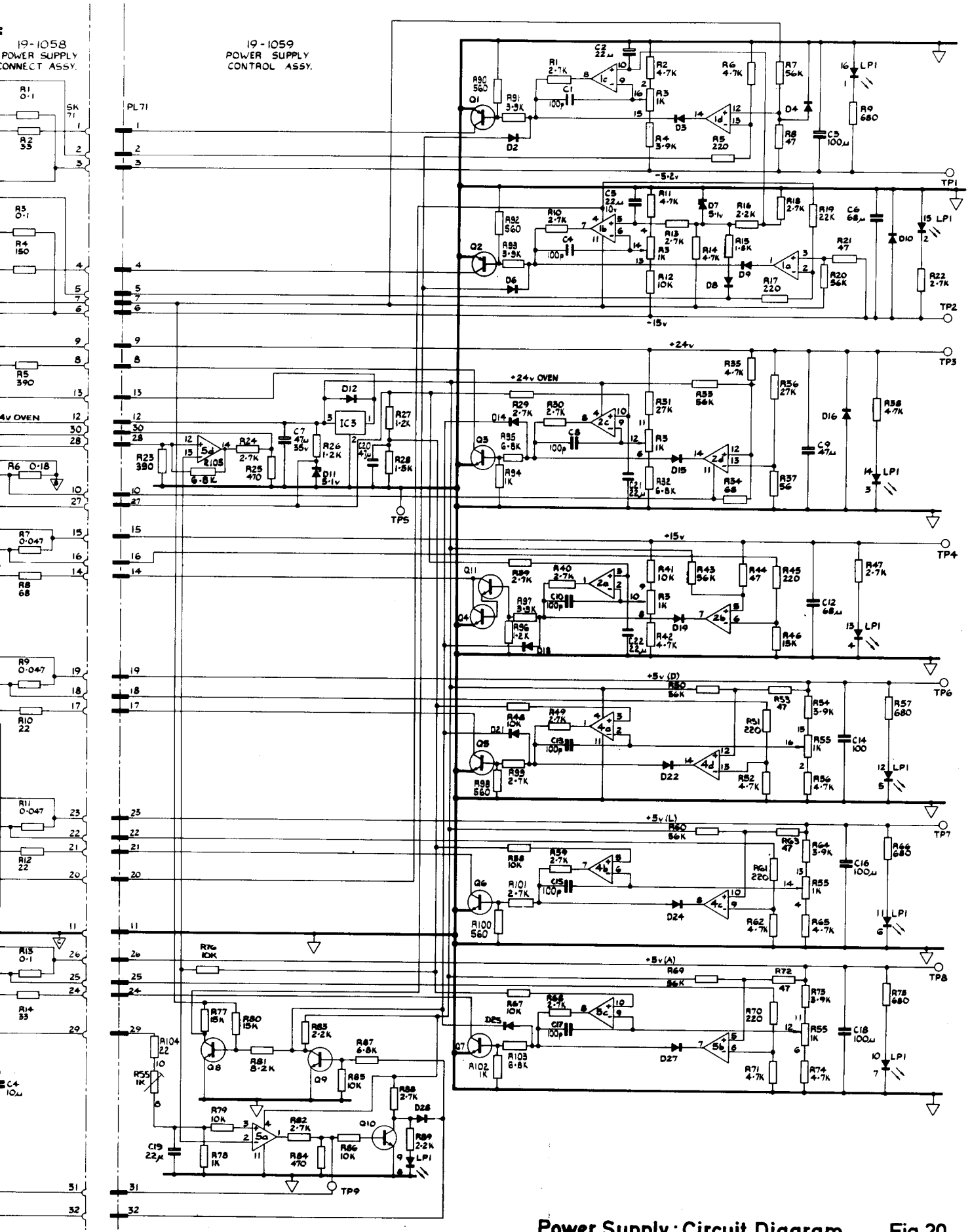
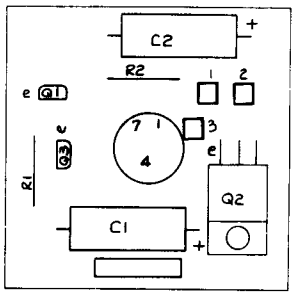
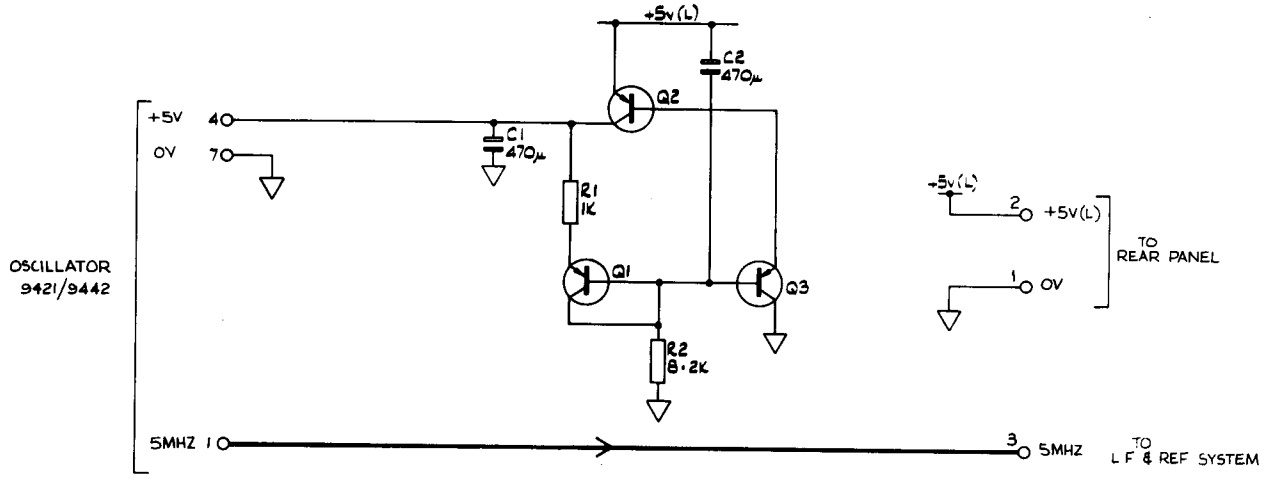
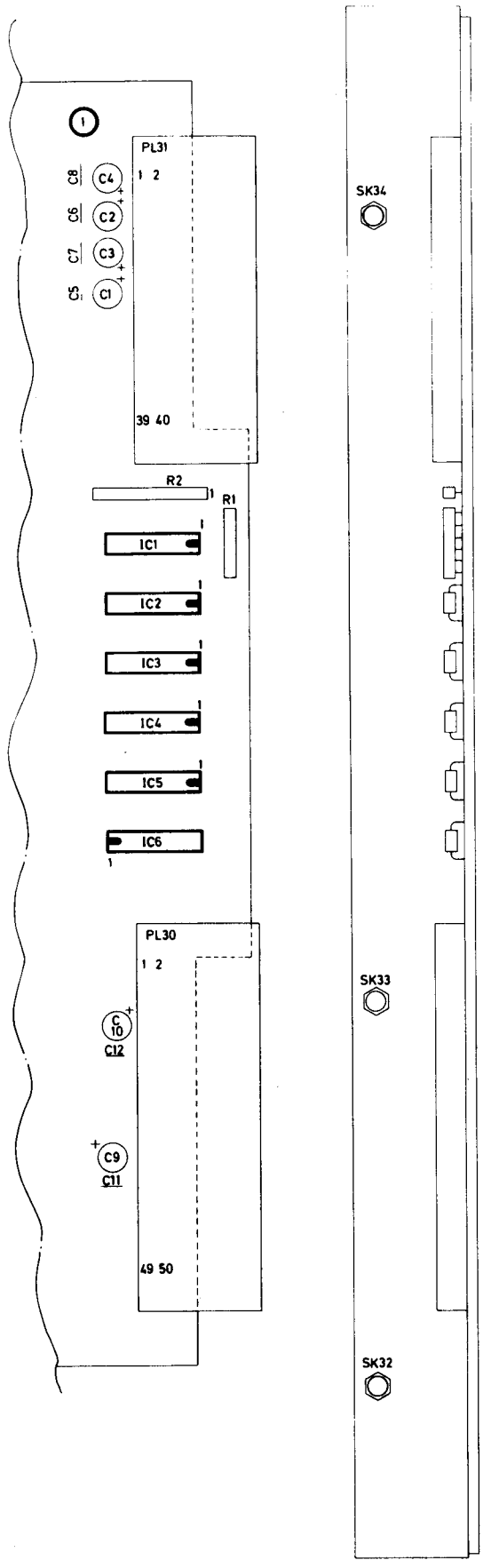


Power Supply : Circuit Diagram Fig.20





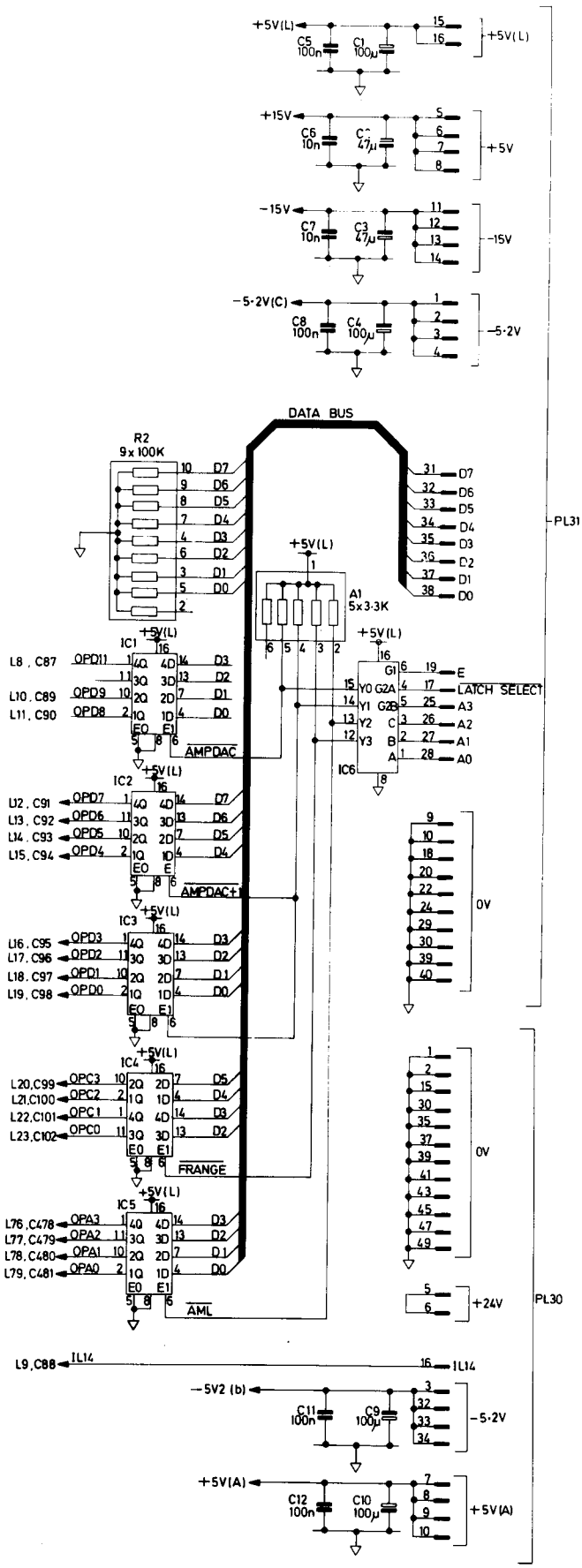
Oscillator Supply Filter Assembly 19-1167 Fig. 21



RACAL
TH3635 19-1044
2

Component Layout :
Output System Module 11-1532

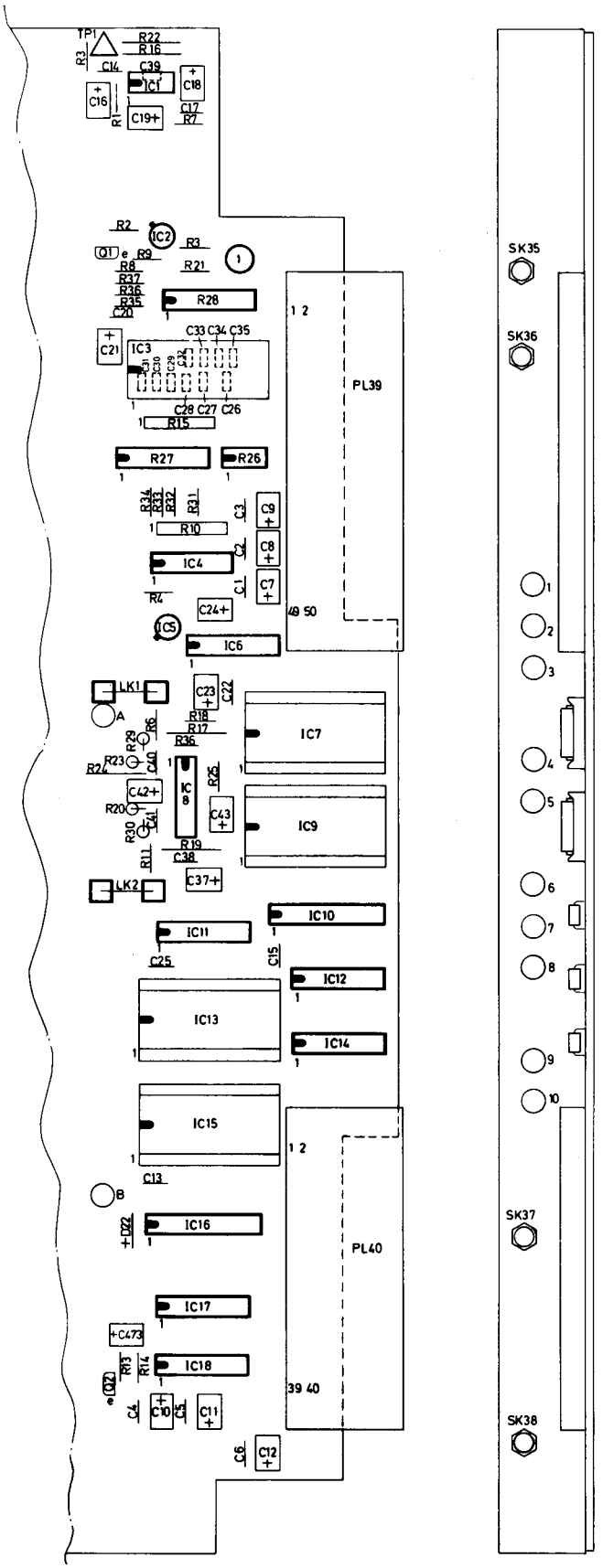
Fig.22



RACAL
TH3635 19-1044
2

Circuit Diagram : Output System Module 11-1532

Fig.23



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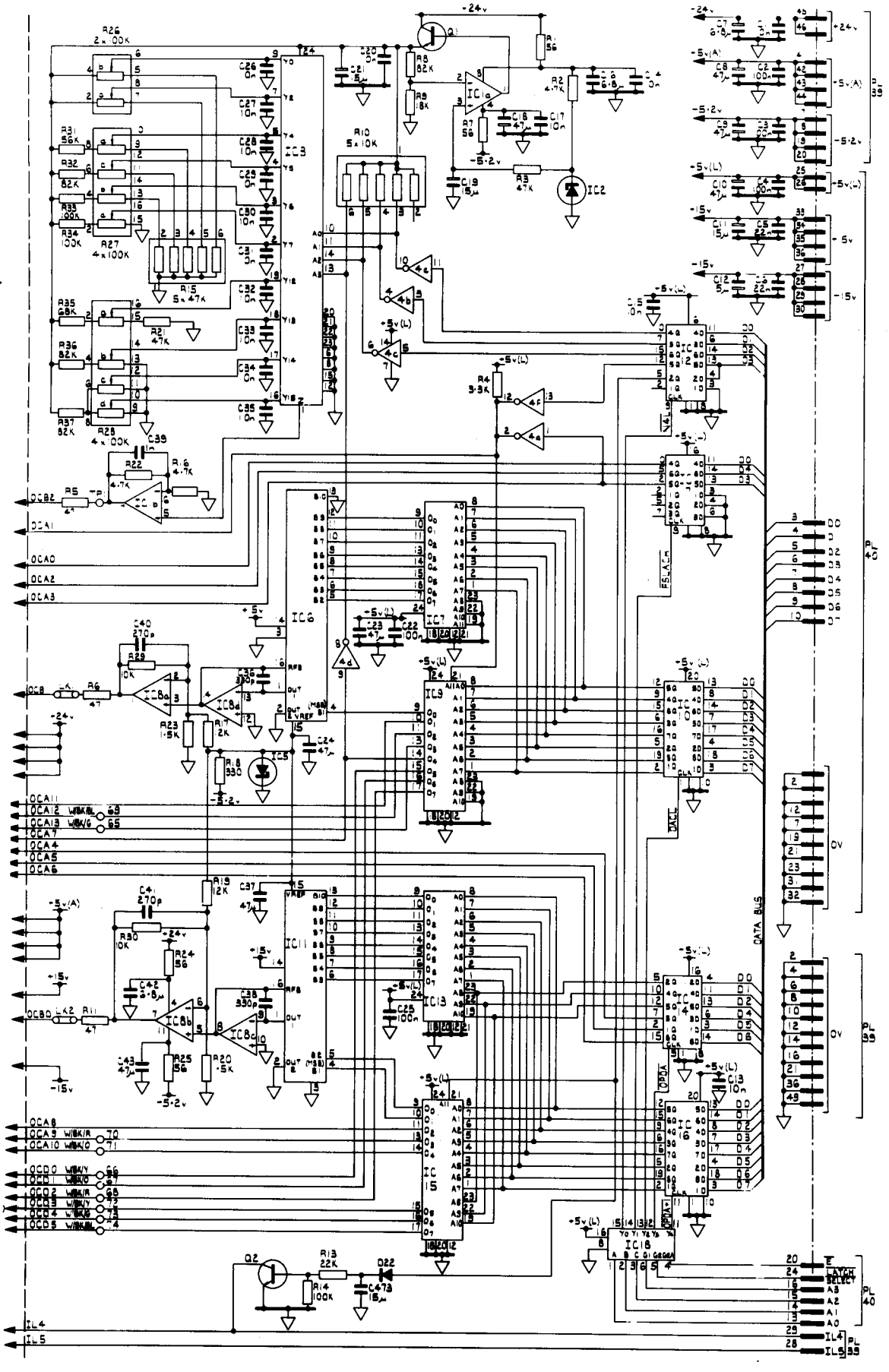
1

Component Layout:
Comb Loop Module 11-1702

Fig. 24



RACAL

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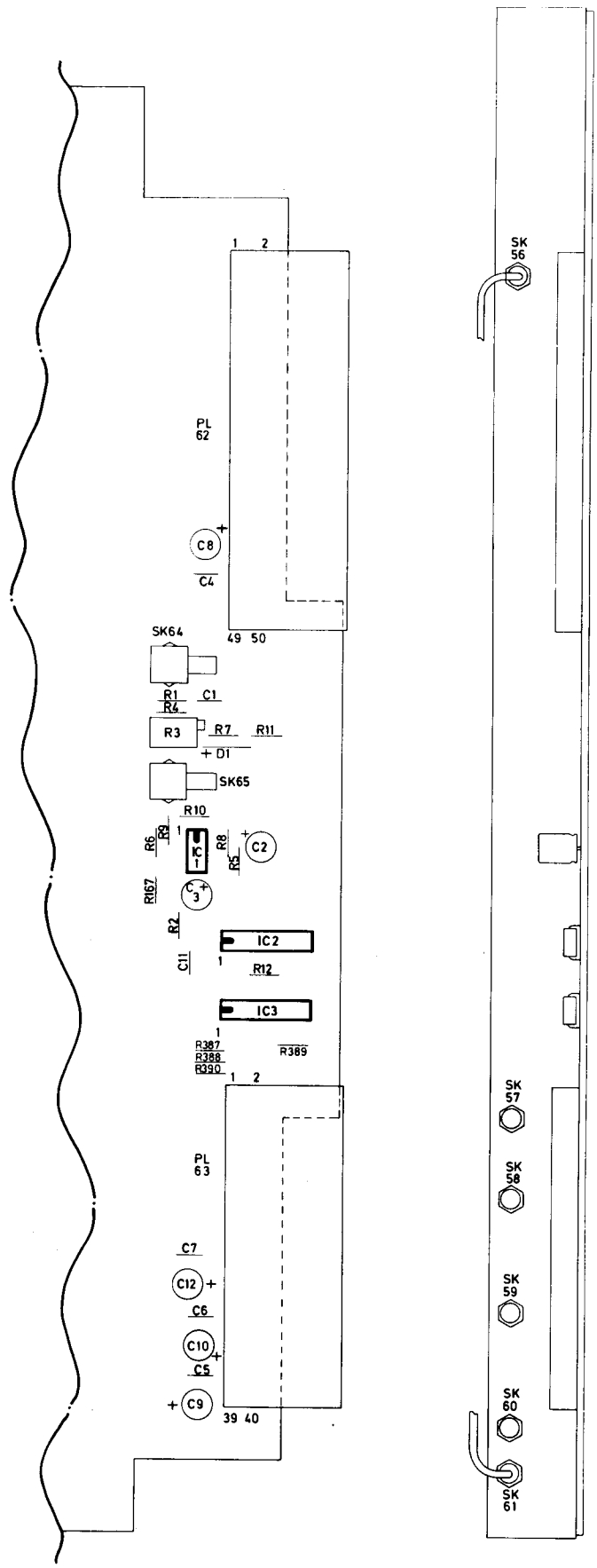
1	

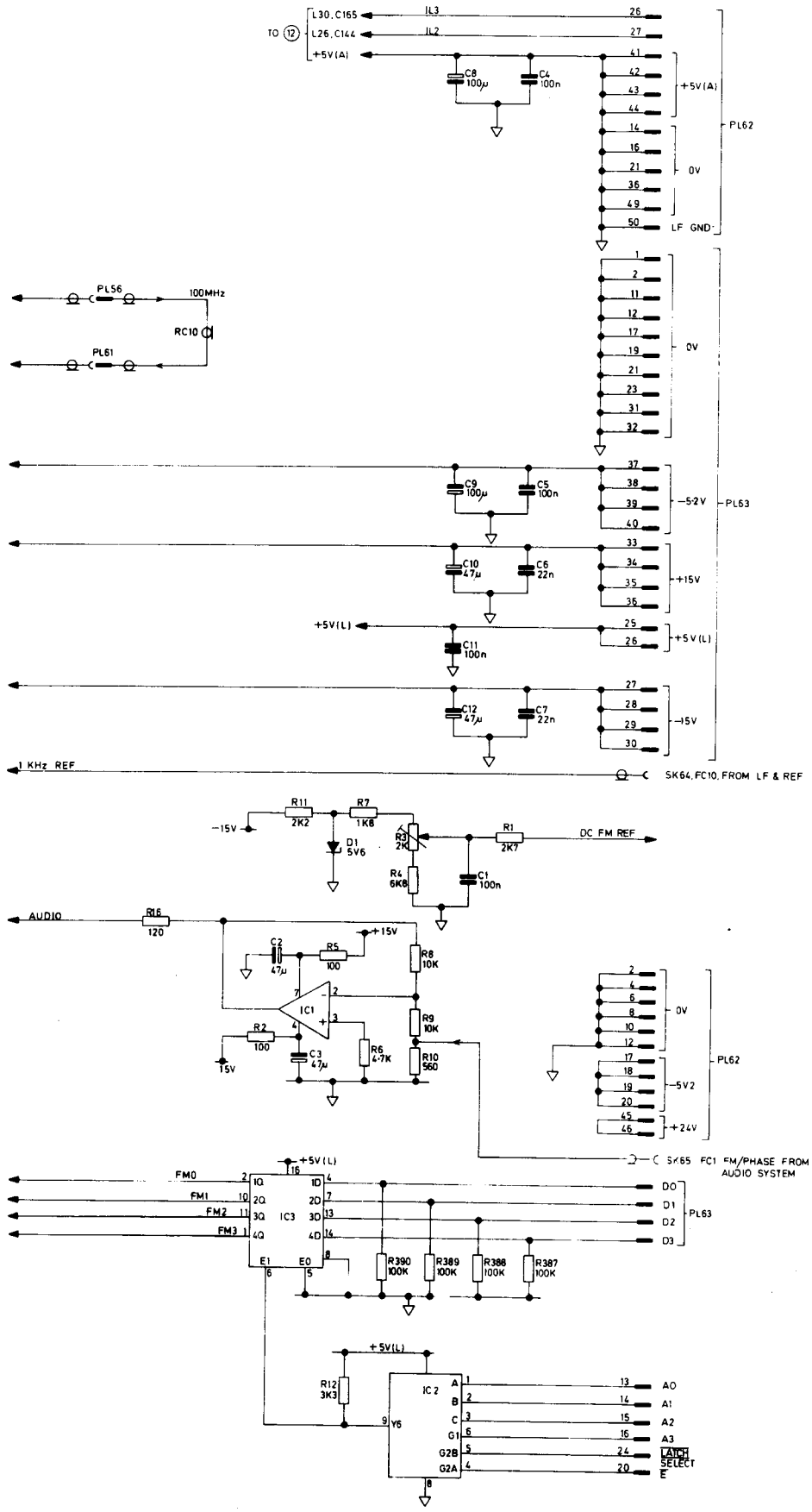
Circuit Diagram: Comb Loop Module 11-1702

Fig.25



RACAL TH3635 19-1046 2

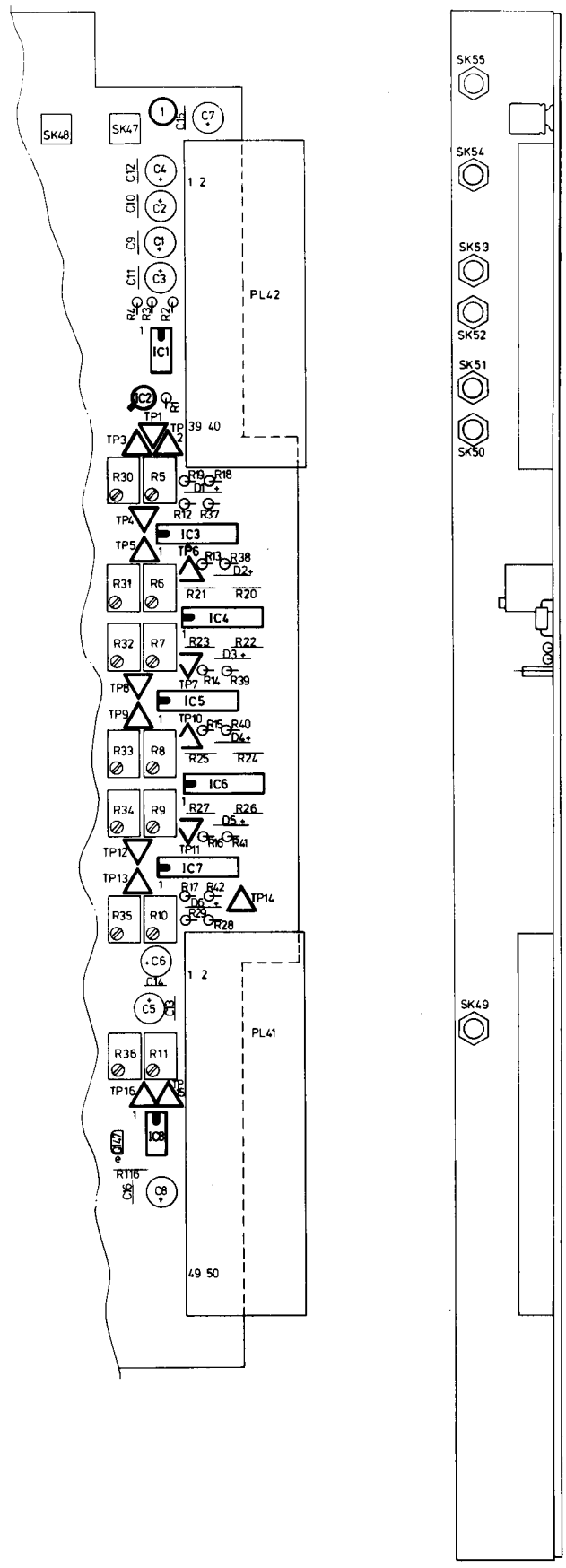
Component Layout : FM System Module 11-1535. Fig.26



RACAL
TH3635 | 19-1046
2

Circuit Diagram: FM System Module 11-1535.

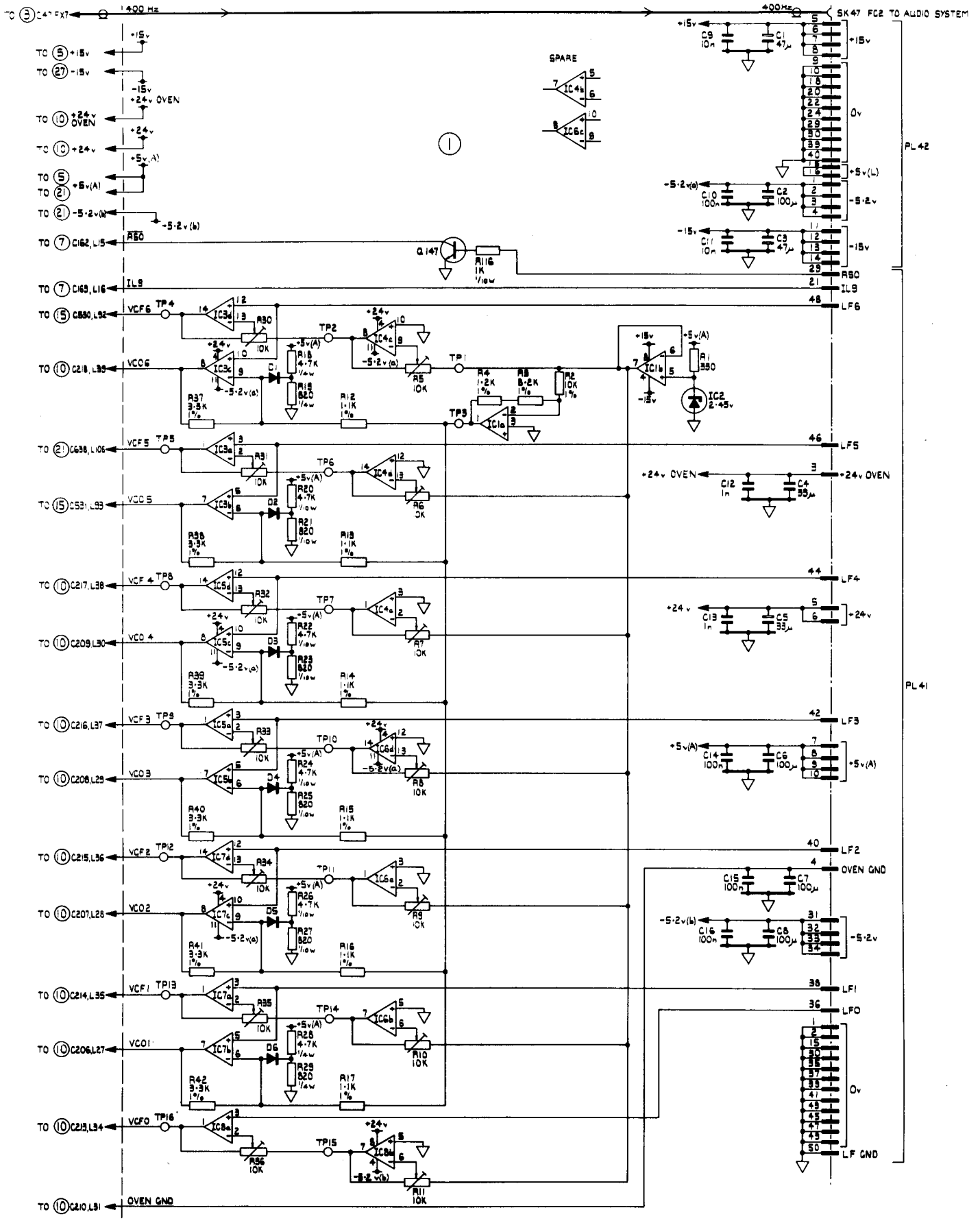
Fig. 27.



RACAL TH3635 | 19-1047 | 3

Component Layout : Reference Generator and LF Synthesizer Module 11-1534.

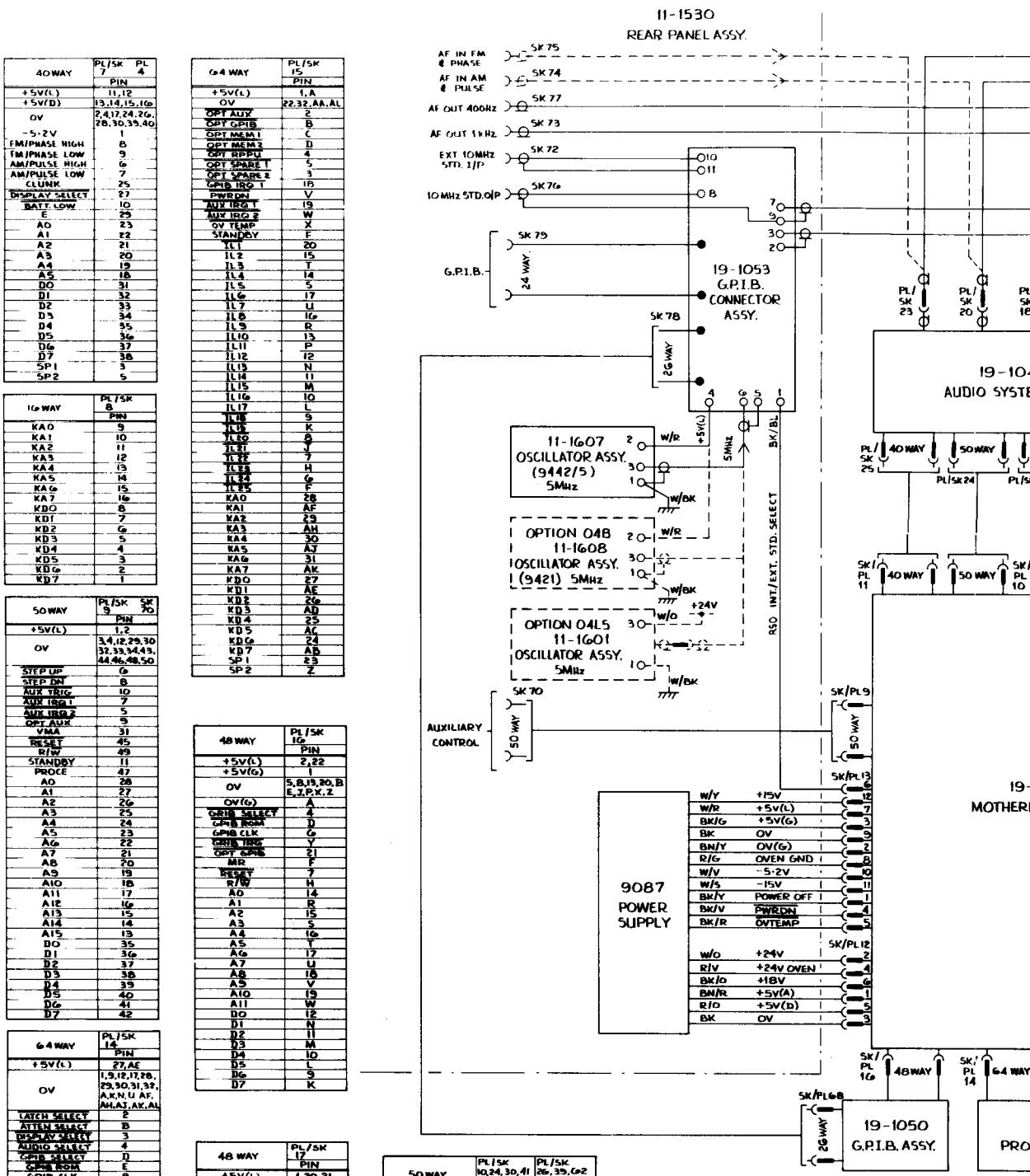
Fig. 28



RACAL
TH3635 | 19-1047
3

Circuit Diagram : Reference Generator and LF Synthesizer Module 11-1534.

Fig. 29



40 WAY	PL/SK 7 4 PIN
+5V(L)	11,12
+5V(D)	13,14,15,16
OV	2,4,17,24,26, 28,30,35,40
-5.2V	1
FM/PHASE HIGH	8
FM/PHASE LOW	9
AM/PULSE HIGH	6
AM/PULSE LOW	7
CLUNK	25
DISPLAY SELECT	27
BATT. LOW	10
E	29
A0	23
A1	22
A2	21
A3	20
A4	19
A5	18
D0	31
D1	32
D2	33
D3	34
D4	35
D5	36
D6	37
D7	38
SP1	3
SP2	5

16 WAY	PL/SK 8 PIN
KA0	9
KA1	10
KA2	11
KA3	12
KA4	13
KA5	14
KA6	15
KA7	16
KD0	8
KD1	7
KD2	6
KD3	5
KD4	4
KD5	3
KD6	2
KD7	1

50 WAY	PL/SK 9 SK 70 PIN
+5V(L)	1,2
OV	3,4,12,29,30 32,33,34,43, 44,46,48,50
STEP UP	6
STEP DN	8
AUX TRIG	10
AUX IRQ 1	7
AUX IRQ 2	5
OPT AUX	9
VMA	31
RESET	45
R/W	49
STANDBY	11
PROCE	47
A0	28
A1	27
A2	26
A3	25
A4	24
A5	23
A6	22
A7	21
A8	20
A9	19
A10	18
A11	17
A12	16
A13	15
A14	14
A15	13
D0	35
D1	36
D2	37
D3	38
D4	39
D5	40
D6	41
D7	42

64 WAY	PL/SK 14 PIN
+5V(L)	27,AE
OV	1,9,12,17,28, 29,30,31,32, A,K,N,U AF, AH,AJ,AK,AL
LATCH SELECT	E
ATTEN SELECT	B
DISPLAY SELECT	3
AUDIO SELECT	4
GPIB SELECT	D
GPIB ROM	E
GPIB CLK	8
MEM 1	F
MEM 2	H
POWVAL	J
MR	11
VMA	10
RESET	M
R/W	L
E	G
E	5
PROCE	7
A0	18
A1	V
A2	19
A3	W
A4	20
A5	X
A6	21
A7	Y
A8	22
A9	Z
A10	23
A11	AA
A12	24
A13	AB
A14	25
A15	AC
D0	16
D1	T
D2	15
D3	S
D4	14
D5	R
D6	13
D7	P

64 WAY	PL/SK 15 PIN
+5V(L)	1,A
OV	22,32,AA,AL
OPT AUX	2
OPT GPIB	B
OPT MEM 1	C
OPT MEM 2	D
OPT SPARE 1	4
OPT SPARE 2	5
GPIB IRQ 1	3
PWRDN	18
AUX IRQ 1	V
AUX IRQ 2	19
OV TEMP	W
STANDBY	X
IL1	E
IL2	20
IL3	15
IL4	T
IL5	14
IL6	5
IL7	17
IL8	U
IL9	16
IL10	R
IL11	13
IL12	P
IL13	12
IL14	N
IL15	11
IL16	M
IL17	10
IL18	L
IL19	9
IL20	K
IL21	8
IL22	J
IL23	7
IL24	H
IL25	G
IL26	F
KA0	28
KA1	AF
KA2	29
KA3	AH
KA4	30
KA5	AJ
KA6	31
KA7	AK
KD0	27
KD1	AE
KD2	26
KD3	AD
KD4	25
KD5	AC
KD6	24
KD7	AB
SP1	23
SP2	Z

48 WAY	PL/SK 16 PIN
+5V(L)	2,22
+5V(G)	1
OV	5,8,13,20,B E,J,P,X,Z
OV(G)	A
GPIB SELECT	4
GPIB ROM	D
GPIB CLK	6
GPIB IRQ	Y
OPT GPIB	21
MR	F
RESET	7
R/W	H
A0	14
A1	R
A2	15
A3	S
A4	16
A5	T
A6	17
A7	U
A8	18
A9	V
A10	19
A11	W
D0	12
D1	N
D2	11
D3	M
D4	10
D5	L
D6	9
D7	K

48 WAY	PL/SK 17 PIN
+5V(L)	1,20,21
OV	3,6,11,A, D,F,M,W
Vcc CMOS	23
MEM 1	B
MEM 2	2
OPT MEM 1	X
OPT MEM 2	19
POWVAL	C
RESET	5
R/W	E
BATT. LOW	Y
BATT. TEST 1	22
BATT. TEST 2	Z
PROCE	4
A0	17
A1	U
A2	16
A3	T
A4	15
A5	S
A6	14
A7	R
A8	13
A9	P
A10	12
A11	N
D0	10
D1	L
D2	9
D3	K
D4	8
D5	J
D6	7
D7	H

50 WAY	PL/SK 10,24,30,41 PIN	PL/SK 26,39,G2 PIN
+24V OVEN	3	48
+24V	5,6	45,46
+5V(A)	7,8,9,10	41,42,43,44
OV	1,2,15,30, 35,37,39,41, 43,45,47,49	2,4,6,8,10, 12,14,16,21, 34,49,50
OVEN GND	4	47
-5.2V	31,32,33,34	17,18,19,20
FM/PHASE HIGH	11	40
FM/PHASE LOW	12	39
AM/PULSE HIGH	13	38
AM/PULSE LOW	14	37
IL2	24	27
IL3	25	26
IL4	22	29
IL5	23	28
IL6	28	23
IL7	27	24
IL8	26	25
IL9	21	30
IL10	20	31
IL11	19	32
IL12	18	33
IL13	17	34
IL14	16	35
LF0	36	15
LF1	38	13
LF2	40	11
LF3	42	9
LF4	44	7
LF5	46	5
LF6	48	3
LF GND	50	1

40 WAY	PL/SK 11,25,31,42 PIN	PL/SK 27,40,G3 PIN
+15V	5,6,7,8	33,34,35,36
+5V(L)	15,16	25,26
OV	9,10,18,20, 22,24,29, 30,34,39	1,2,11,12,17 19,21,23, 31,32
-5.2V	1,2,3,4	37,38,39,40
-15V	11,12,13,14	27,28,29,30
LATCH SELECT	17	24
AUDIO SELECT	23	18
E	19	22
E	21	20
A0	28	13
A1	27	14
A2	26	15
A3	25	16
D0	38	3
D1	37	4
D2	36	5
D3	35	6
D4	34	7
D5	33	8
D6	32	9
D7	31	10

26 WAY	PL/SK G8 76 PIN
OV	2,3,4,11
NDAC	15
DAV	17
NRFD	16
REN	1
SRQ	13
ATN	12
IFC	14
EOI	18
AS1	10
AS2	9
AS3	8
AS4	7
AS5	6
LISTEN ONLY	5
DIO1	22
DIO2	21
DIO3	20
DIO4	19
DIO5	23
DIO6	24
DIO7	25
DIO8	26

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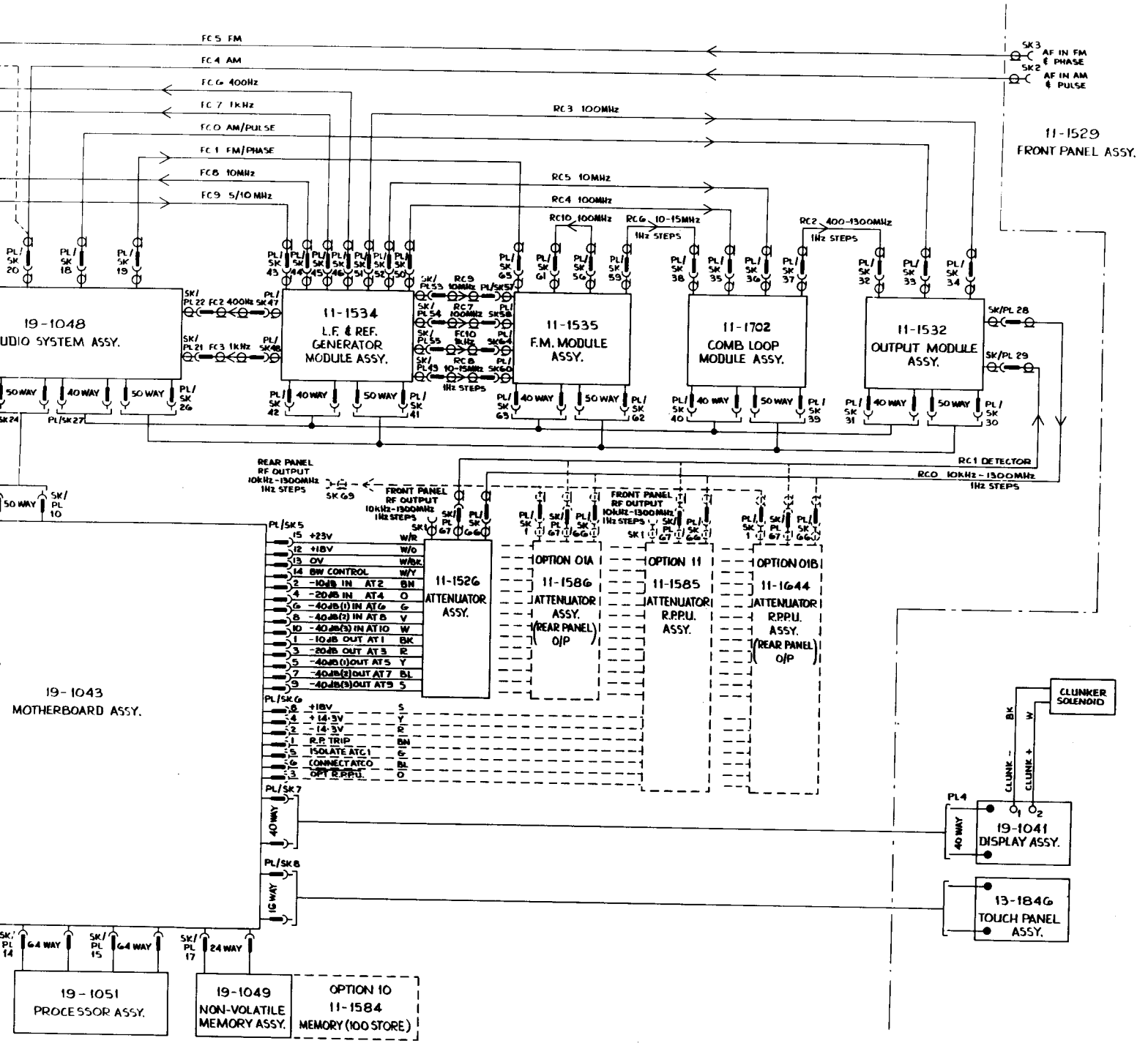
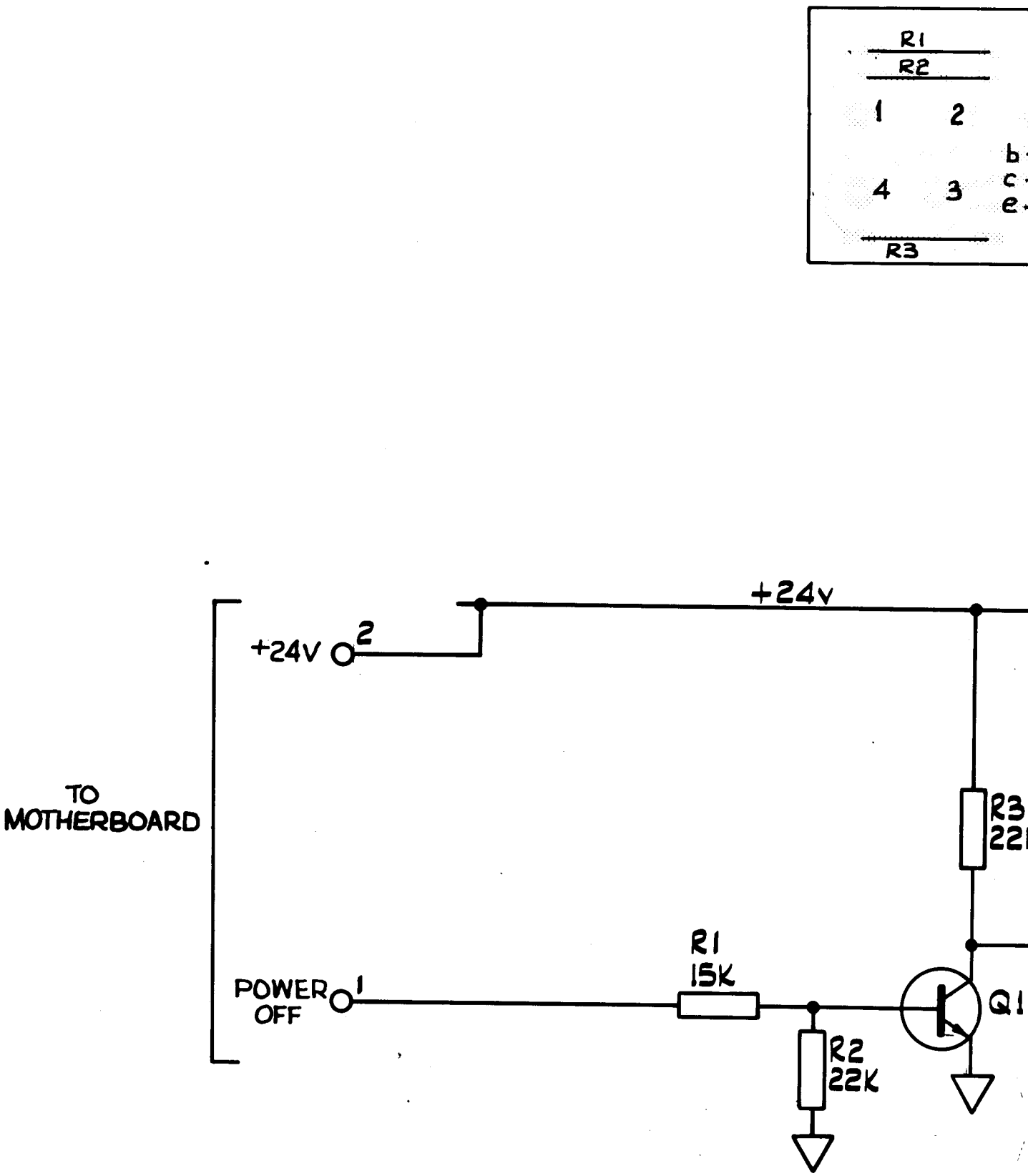


PL/SK 68 PIN	SK 78
2,3,4,11	
15	
17	
16	
1	
13	
12	
14	
18	
10	
9	
8	
7	
6	
5	
22	
21	
20	
19	
23	
24	
25	
26	

24 WAY	SK 79 PIN
0V	12,18,19,20, 21,22,23,24
NDAC	8
DAV	6
NRFD	7
REN	17
SRQ	10
ATN	11
IFC	9
EOI	5
DIO1	1
DIO2	2
DIO3	3
DIO4	4
DIO5	13
DIO6	14
DIO7	15
DIO8	16

Interconnections **Fig. 30**



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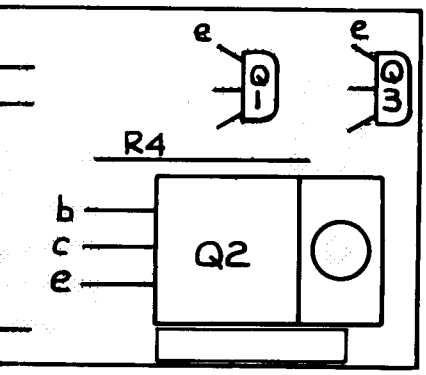

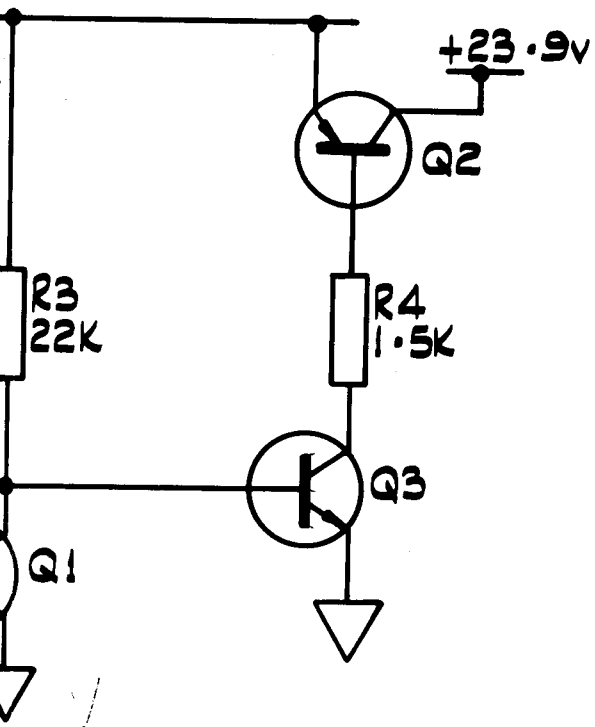

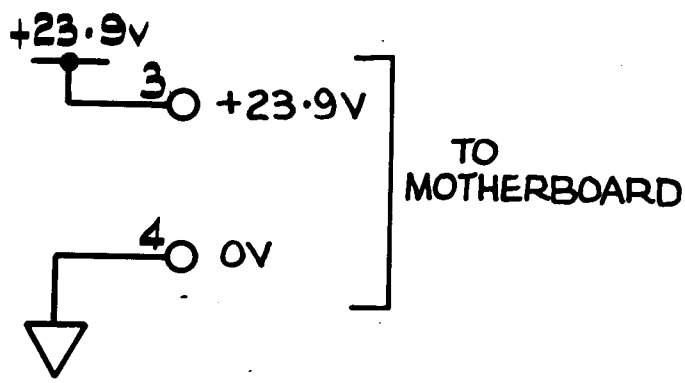

Austron Oscillator Option :
Supply Switching Assembly 19-1158. Fig 31

Racal-Dana Instruments

September 1984

SYNTHESIZED SIGNAL GENERATOR 9087

AMENDMENT

The following manuscript amendment should be made to the Issue 1 Maintenance Manual:

PAGE 3-2

Paragraph 3.4.1	Delete 'pin 30' Insert 'pin 27'

PAGE 4-5

Auxiliary Control Socket	Delete '30' Insert '27'

Racal-Dana Instruments October 1984

SYNTHESIZED SIGNAL GENERATOR 9087

AMENDMENT

The following manuscript amendment should be made to the Issue 1 Maintenance Manual.

PARTS LIST 57

Resistors	R10	Delete 'Carbon Film 0.1 5 20-1536'	
		Insert 'Metal Film 1/4 1 20-4880'	

PAGE 6-33

Paragraph 6.5.11.1 Delete 'Fig.22' Insert 'Fig.23'

PAGE 6-34

Paragraph 6.5.12.1.1 Delete 'Fig.24' Insert 'Fig.25'.

CN12836
9087
Issue 1
Amendment No.2

SYNTHESIZED SIGNAL GENERATOR 9087

The changes listed below have been made to some instruments having serial numbers above 1250.

Changes found to apply to the instrument with which this manual is to be used should be incorporated in the manual by manuscsript amendment.

PAGE 3-1

Paragraph 3.2.2.1 Delete '1/4in x 1 1/4in' '23-0061' and '23-0036'
Insert '5mm x 20mm' '23-0064' and '23-0021'.

PAGE 4-5

Paragraph 4.2.3, Line Fuse Delete '1/4in x 1 1/4in'
Insert '5mm x 20mm'

PARTS LIST 41

Power Input Connector	Delete '23-3294'	Insert '23-3420'
	Delete '23-0061'	Insert '23-0064'
	Delete '23-0036'	Insert '23-0021'